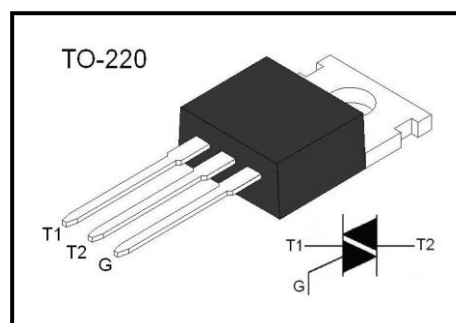


Applications

- General purpose switching and phase control
- 230V lamp dimmers

Features

- Very sensitive gate
- Gate triggering in four quadrants
- Direct interfacing to logic level lcs
- Direct interfacing to low power gate drive circuits



Absolute Maximum Ratings

Limiting values in accordance with the Absolute Maximum System (IEC 134).

Parameter	Symbol	Conditions		Ratings	Unit
Repetitive peak off-state voltages	V_{DRM}, V_{RRM}			600 800	V
On-State RMS Current	$I_{T(RMS)}$	full sine wave; $T_{mb} \leq 99^\circ\text{C}$		12	A
Non-repetitive peak on-state current	I_{TSM}	full sine wave; $T_j = 25^\circ\text{C}$ prior to surge	$t = 20\text{ ms}$	95	A
			$t = 16.7\text{ ms}$	105	
I^2t for fusing	I^2t	$t = 10\text{ ms}$		45	A^2s
Repetitive rate of rise of on-state current after triggering	di/dt	$I_{TM} = 20\text{A}; I_G = 0.2\text{A};$ $di_G/dt = 0.2\text{A}/\mu\text{s}$	T2+ G+	50	$\text{A}/\mu\text{s}$
			T2+ G-	50	
			T2- G-	50	
			T2- G+	10	
Peak gate current	I_{GM}			2	A
Peak Gate Voltage	V_{GM}			5	V
Peak gate power	P_{GM}			5	W
Average gate power	$P_{G(AV)}$	over any 20 ms period		0.5	W
Operating junction temperature	T_j			-40 ~ 125	$^\circ\text{C}$
Storage Temperature	T_{stg}			-40 ~ 150	$^\circ\text{C}$

Thermal Resistances

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Thermal resistance junction to mounting base	$R_{th\ j-mb}$	full cycle half cycle	-		1.5 2.0	K/W
Thermal resistance junction to ambient	$R_{th\ j-a}$	pcb mounted; minimum footprint pcb mounted;	-	60		K/W

Static Characteristics $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Gate trigger current	I_{GT}	$V_D = 12\text{ V}, I_T = 0.1\text{ A}$	T2+ G+	-	10	mA
			T2+ G-	-	10	
			T2- G-	-	10	
			T2- G+	-	25	
Latching current	I_L	$V_D = 12\text{ V}, I_T = 0.1\text{ A}$	T2+ G+	-	30	mA
			T2+ G-	-	40	
			T2- G-	-	30	
			T2- G+	-	40	
Holding current	I_H	$V_D = 12\text{ V}, I_{GT} = 0.1\text{ A}$			30	mA
On-state voltage	V_T	$I_T = 15\text{ A}$			1.65	V
Gate trigger voltage	V_{GT}	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$			1.5	V
		$V_D = 400\text{ V}; I_T = 0.1\text{ A}; T_j = 125\text{ }^{\circ}\text{C}$	0.25			
Off-state leakage current	I_D	$V_D = V_{DRM(max)}; T_j = 125\text{ }^{\circ}\text{C}$		0.1	0.5	mA

Dynamic Characteristics $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Critical rate of rise of off-state voltage	dV_D/dt	$V_{DM} = 67\% V_{DRM(max)};$ $T_j = 125\text{ }^{\circ}\text{C};$ exponential waveform; gate open circuit		150		V/ μs
Gate controlled turn-on time	t_{gt}	$I_{TM} = 16\text{ A}; V_D = V_{DRM(max)};$ $I_G = 0.1\text{ A}; dI_G/dt = 5\text{ A}/\mu\text{s}$		2		μs

Typical Characteristics

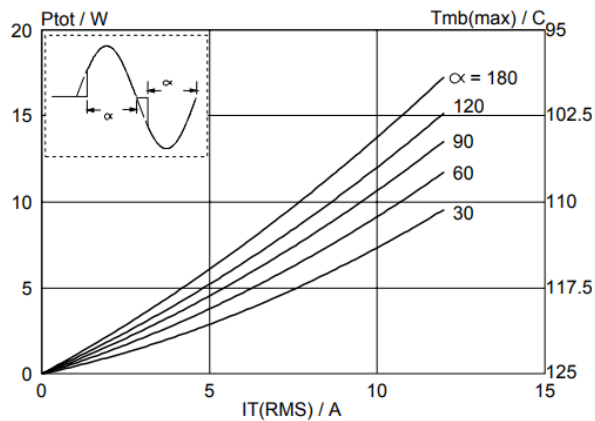


Fig.1. Maximum on-state dissipation, P_{tot} , versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

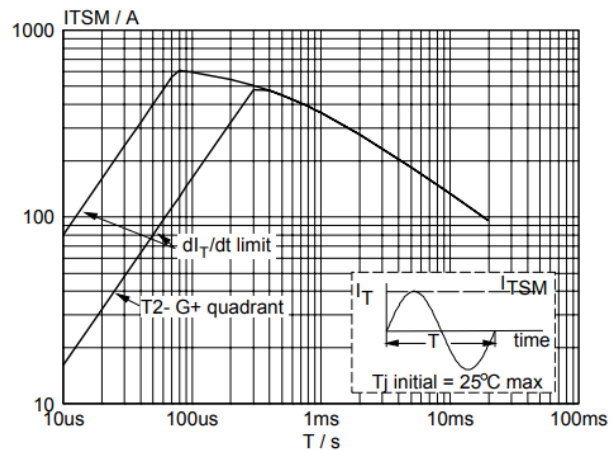


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus pulse width t_p , for sinusoidal currents, $t_p \leq 20$ ms.

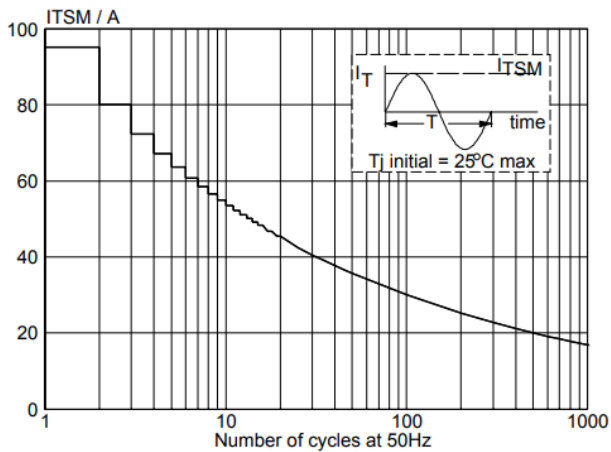


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus number of cycles, for sinusoidal currents, $f = 50$ Hz.

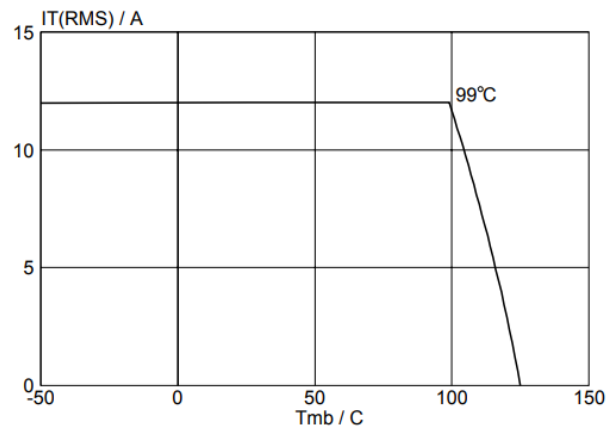


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus lead temperature T_{lead} .

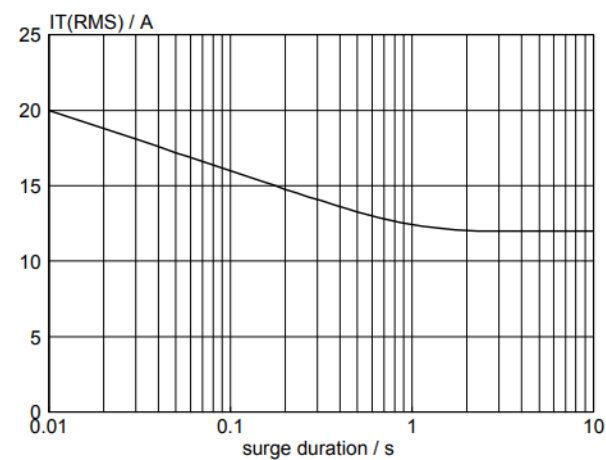


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, $f = 50$ Hz; $T_{mb} \leq 99^\circ\text{C}$.

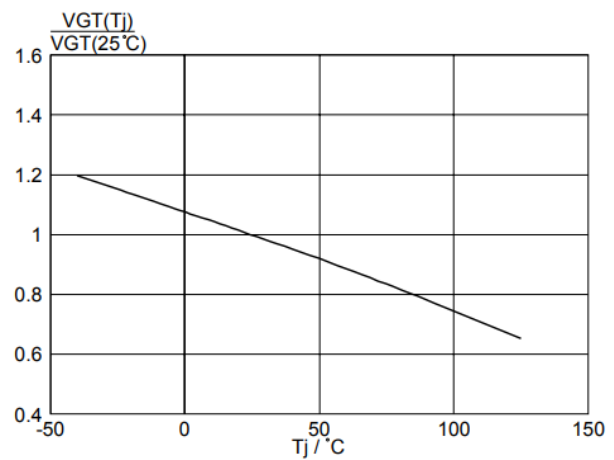


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j) / V_{GT}(25^\circ\text{C})$, versus junction temperature T_j .

Typical Characteristics

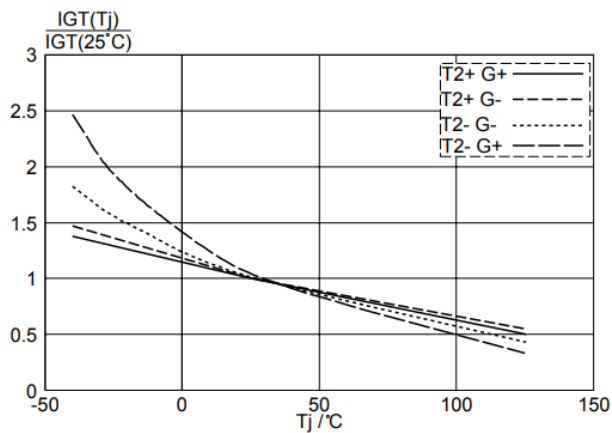


Fig.7. Normalised gate trigger current $I_{GT}(T_j) / I_{GT}(25^\circ\text{C})$, Versus junction temperature T_j .

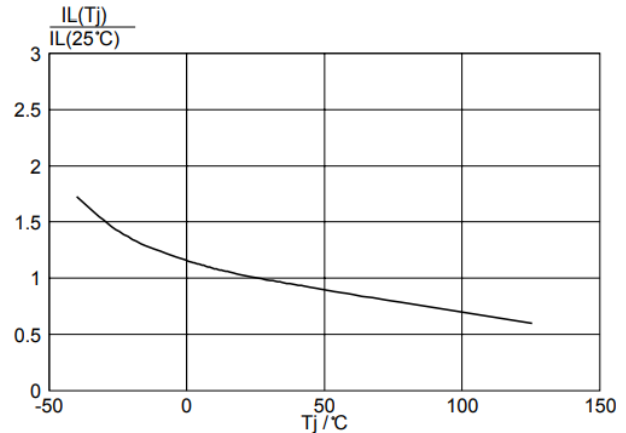


Fig.8. Normalised latching current $I_L(T_j) / I_L(25^\circ\text{C})$, versus junction temperature T_j .

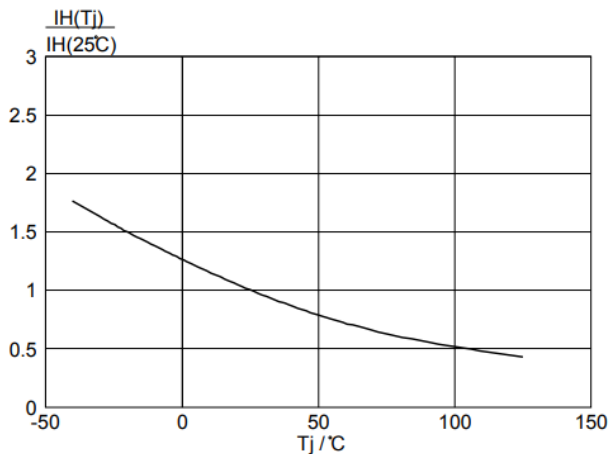


Fig.9. Normalised holding current $I_H(T_j) / I_H(25^\circ\text{C})$, versus junction temperature T_j .

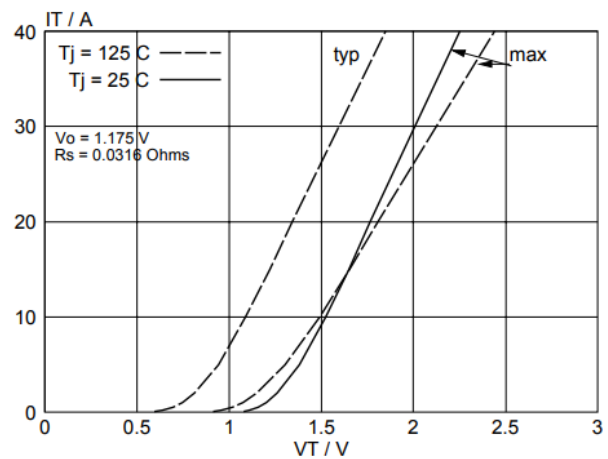


Fig.10. Typical and maximum on-state characteristic.

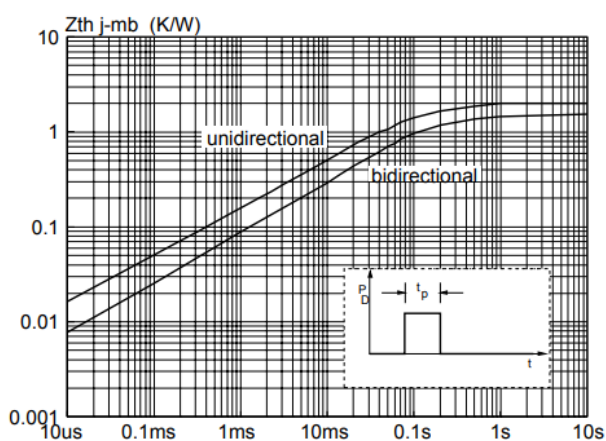


Fig.11. Transient thermal impedance $Z_{th} j\text{-lead}$, versus pulse width t_p .

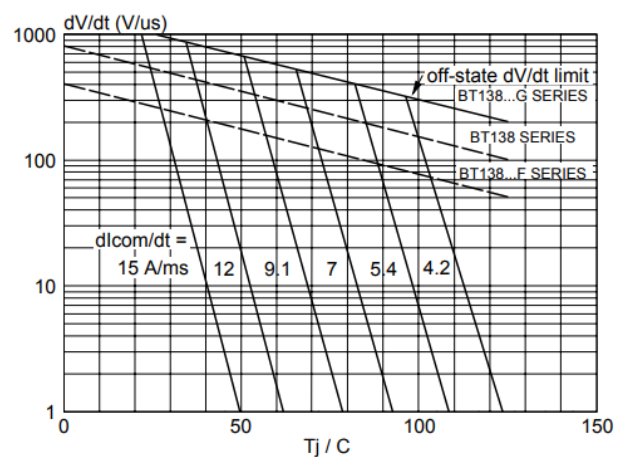


Fig.12. Typical, critical rate of rise of off-state voltage, dV/dt versus junction temperature T_j .

Package Dimensions

Dim	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	4.34	4.67	0.171	0.184
A1	2.52	2.82	0.099	0.111
b	0.71	0.91	0.028	0.036
b1	1.17	1.37	0.046	0.054
c	0.30	0.50	0.012	0.020
c1	1.17	1.37	0.046	0.054
D	9.90	10.20	0.390	0.402
E	8.50	8.90	0.335	0.350
E1	12.00	12.50	0.472	0.492
e	2.44	2.64	0.096	0.104
e1	4.88	5.28	0.192	0.208
F	2.60	2.80	0.102	0.110
L	13.20	13.80	0.520	0.543
L1	3.80	4.20	0.150	0.165
Φ	3.60	3.96	0.142	0.156