TEXAS INSTRUMENTS

TLC320AD50C/I
TLC320AD52C

Sigma-Delta Analog Interface Circuits With Master-Slave Function

Data Manual

2000

Mixed Signal Products

SLAS131E

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1 Introduction

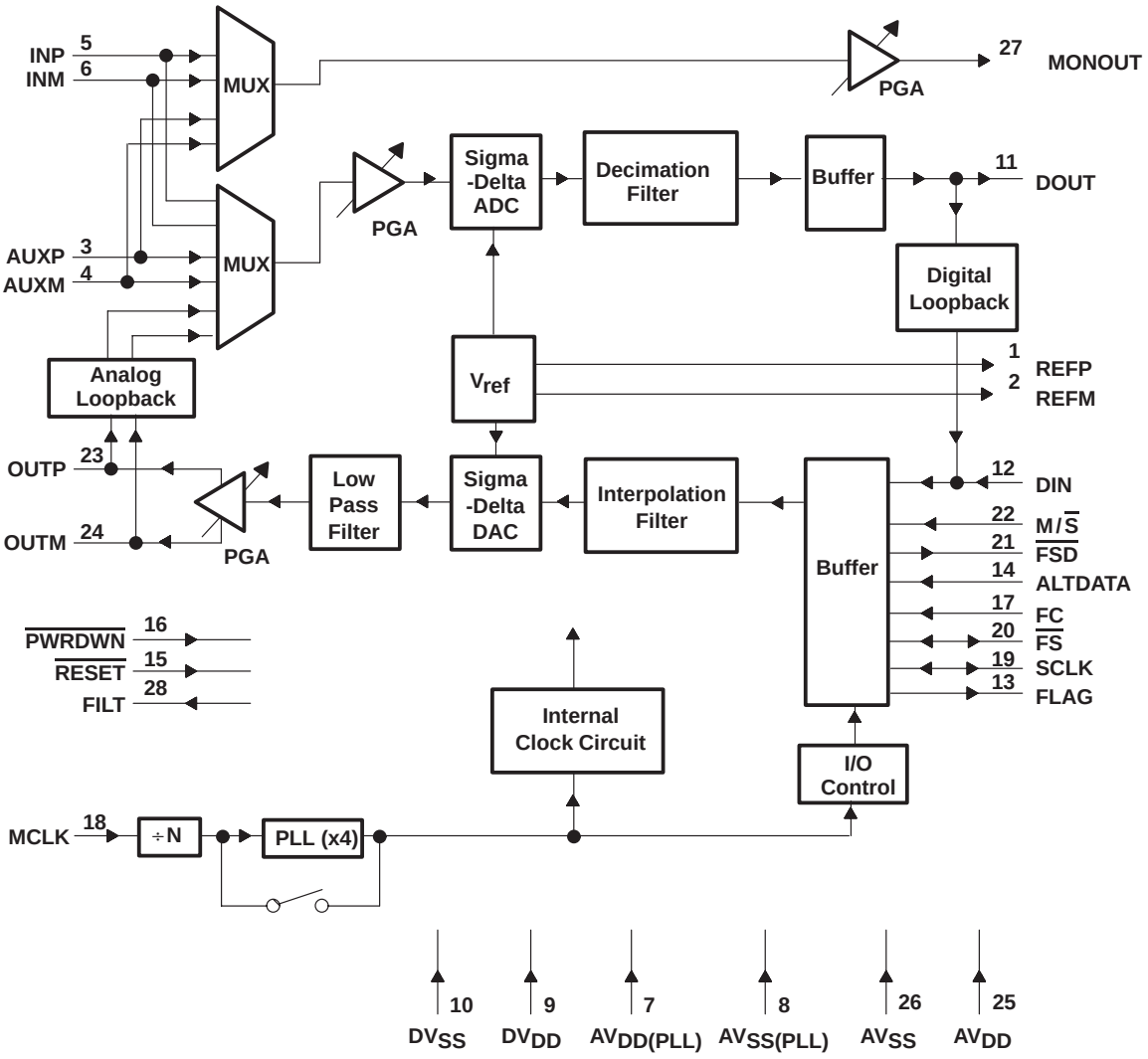
The TLC320AD50C, TLC320AD50I, and TLC320AD52C provide high-resolution signal conversion from digital-to-analog (D/A) and from analog-to-digital (A/D) using oversampling sigma-delta technology. This device consists of a pair of 16-bit synchronous serial conversion paths (one for each direction) and includes an interpolation filter before the DAC and a decimation filter after the ADC. Other overhead functions on the chip include timing (sample rate, $\overline{\text{FSD}}$ delay) and control (programmable gain amplifier, PLL, communication protocol, etc.). The sigma-delta architecture produces high resolution A/D and D/A conversion at a low system cost.

Programmable functions of this device can be selected through the serial interface. Options include reset, power down, communications protocol, signal sampling rate, gain control, and system test modes (see section 6). The TLC320AD50C and TLC320AD52C are characterized for operation from 0°C to 70°C, and the TLC320AD50I is characterized for operation from –40°C to 85°C.

1.1 Features

- General-purpose analog interface circuit for V.34+ modem and business audio applications
- 16-bit oversampling sigma-delta ADC and DAC
- Serial port interface
- Typical 89-dB SNR (signal-to-noise ratio) for ADC and DAC
- Typical 90-dB THD (signal to total harmonic distortion) for ADC and DAC
- Typical 88-dB dynamic range
- Test mode that includes a digital loopback test and analog loopback test
- Programmable A/D and D/A conversion rate
- Programmable input and output gain control
- Maximum conversion rate: 22.05 kHz
- Single 5-V power supply voltage or 5-V analog and 3-V digital power supply voltage
- Power dissipation (P_D) of 120 mW rms typical in the operating mode
- Hardware power-down mode to 7.5 mW
- Internal reference voltage (V_{ref})
- Differential architecture throughout device
- TLC320AD50C/I can support up to three slave devices; TLC320AD52C can support one slave
- 2s complement data format
- ALTDATA terminal provides data monitoring
- Monitor amplifier to monitor input signals
- On-chip phase locked loop (PLL)

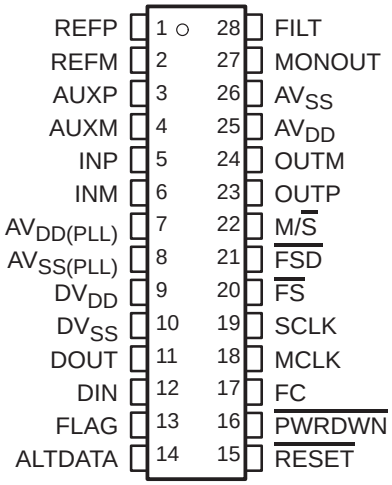
1.2 Functional Block Diagram



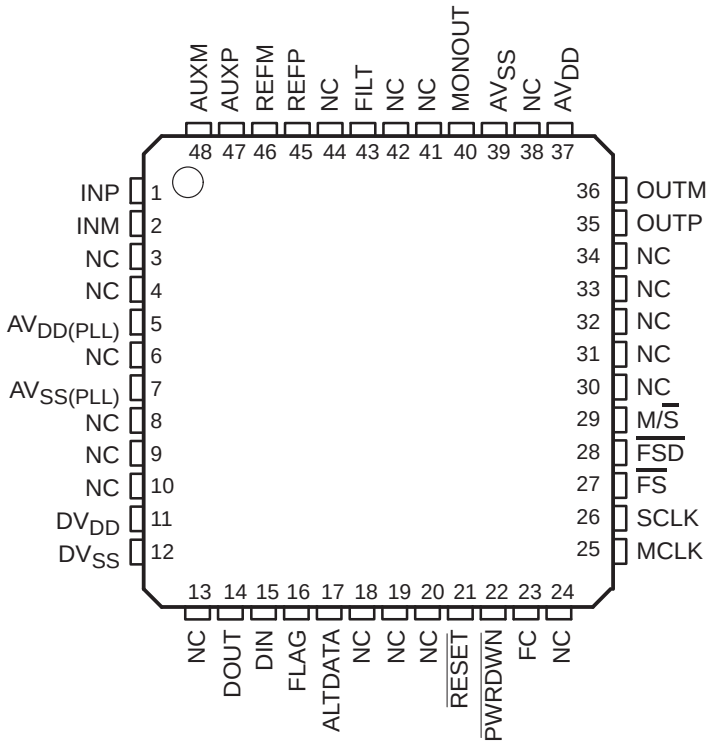
NOTE: Pin numbers shown are for the DW package.

1.3 Terminal Assignments

DW PACKAGE
(TOP VIEW)



PT PACKAGE
(TOP VIEW)



NC – No internal connection

1.4 Ordering Information

T_A	PACKAGE	
	SMALL OUTLINE PLASTIC DIP (DW)	QUAD FLAT PACK (PT)
0°C to 70°C	TLC320AD50CDW TLC320AD52CDW	TLC320AD50CPT TLC320AD52CPT
–40°C to 85°C	TLC320AD50IDW	

1.5 Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO. PT	NO. DW		
ALTDATA	17	14	I	Alternate data. ALTDATA signals are routed to DOUT during secondary communication if the phone mode is enabled using control 2 register.
AUXM	48	4	I	Inverting input to auxiliary analog input. AUXM requires an external single-pole antialias filter with a low output impedance and should be tied to AV_{SS} if not used.
AUXP	47	3	I	Noninverting input to auxiliary analog input. AUXP requires an external single-pole antialias filter with a low output impedance and should be tied to AV_{SS} if not used.
AV_{DD}	37	25	I	Analog ADC power supply (5 V only) (see Note 1)
$AV_{DD(PLL)}$	5	7	I	Analog power supply for the internal PLL (5 V only) (see Note 1)
AV_{SS}	39	26	I	Analog ground (see Note 1)
$AV_{SS(PLL)}$	7	8	I	Analog ground for the internal PLL (see Note 1)
DIN	15	12	I	Data input. DIN receives the DAC input data and register data from the external DSP (digital signal processor) and is synchronized to SCLK and $\overline{FS}$. Data is latched at the falling edge of SCLK when $\overline{FS}$ is low. DIN is at high impedance when $\overline{FS}$ is not active.
DOUT	14	11	O	Data output. DOUT transmits the ADC output bits and register data, and is synchronized to SCLK. Data is sent out at the rising edge of SCLK when $\overline{FS}$ is low. DOUT is at high impedance when $\overline{FS}$ is not activated. When configured as a master, DOUT is active only during the appropriate time slot. DOUT is in high impedance during the frame syncs for the slaves.
DV_{DD}	11	9	I	Digital power supply (5 V or 3 V) (see Note 1)
DV_{SS}	12	10	I	Digital ground (see Note 1)
FC	23	17	I	Hardware secondary communication request. When FC is set to high, a secondary communication, followed by the primary communication, will occur to transfer data between this device and the external controller. FC is sampled and latched on the rising edge of $\overline{FS}$ at the end of the primary serial communication. See section 3 for details.
FILT	43	28	O	Bandgap filter. FILT is provided for decoupling of the bandgap reference, and provides 3.2 V. The optimal capacitor value is 0.1 μF (ceramic). This voltage node should be loaded only with a high-impedance dc load.
FLAG	16	13	O	Output flag. During phone mode, FLAG contains the value set in control 2 register.
$\overline{FS}$	27	20	I/O	Frame sync. $\overline{FS}$ is an output when the device is configured as a master (M/$\overline{S}$ pin tied high). $\overline{FS}$ is an input when the device is configured as a slave (M/$\overline{S}$ pin tied low). When configured as a slave, data will transfer when $\overline{FS}$ goes low. $\overline{FS}$ is internally generated in the master mode for the master device and all slave devices. In the master mode $\overline{FS}$ is low during data transfer.
$\overline{FSD}$	28	21	O	Frame sync delayed output. The $\overline{FSD}$ (active-low) output synchronizes a slave device to the frame sync of the master device. $\overline{FSD}$ is applied to the slave $\overline{FS}$ input and is the same duration as the master $\overline{FS}$ signal but is delayed in time by the number of shift clocks programmed in the control 3 register.
INM	2	6	I	Inverting input to analog modulator. INM requires an external single-pole antialias filter with a low output impedance.
INP	1	5	I	Noninverting input to analog modulator. INP requires an external single-pole antialias filter with a low output impedance.

NOTES: 1. Separate analog and digital power and ground pins are supplied on this device. For best operation and results, the PC board designer should utilize separate analog and digital power supplies as well as separate analog and digital ground planes.
2. All digital inputs and outputs are TTL compatible, unless otherwise noted (for DV_{DD} = 5 V).

1.5 Terminal Functions (Continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO. PT	NO. DW		
M/$\overline{S}$	29	22	I	Master/slave select input. When M/$\overline{S}$ is high, the device is the master. When M/$\overline{S}$ is low, the device is a slave.
MCLK	25	18	I	Master clock. MCLK derives the internal clocks of the sigma-delta analog interface circuit.
MONOUT	40	27	O	Monitor output. MONOUT allows for monitoring of the analog input and is a high-impedance output. The gain or mute is selected using control 1 register.
OUTM	36	24	O	Inverting output of the DAC. The OUTM output can be loaded with 600 Ω. OUTM is functionally identical with and complementary to OUTP. OUTM can also be used alone for single-ended operation.
OUTP	35	23	O	Noninverting output of the DAC. The OUTP output can be loaded with 600 Ω. OUTP can also be used alone for single-ended operation.
$\overline{PWRDWN}$	22	16	I	Power down. When $\overline{PWRDWN}$ is pulled low, the device goes into a power-down mode, the serial interface is disabled. However, all the register values are sustained and the device resumes full power operation without reinitialization when $\overline{PWRDWN}$ is pulled high again. $\overline{PWRDWN}$ resets the counters only and preserves the programmed register contents (see paragraph 2.2.2 for more information).
REFM	46	2	O	Voltage reference filter output. REFM is provided for low-pass filtering of the internal bandgap reference. The optimal ceramic capacitor value is 0.1 μF and should be connected between REFM and REFP. DC voltage at REFM is 0 V.
REFP	45	1	O	Voltage reference filter positive output. REFP is provided for low-pass filtering of the internal bandgap reference. The optimal ceramic capacitor value is 0.1 μF and should be connected between REFP and REFM. DC voltage at REFP is 3.2 V.
$\overline{RESET}$	21	15	I	Reset. $\overline{RESET}$ initializes all of the internal registers to their default values. The serial port can be configured to the default state accordingly. See section 6 and paragraph 2.2.1 for more information.
SCLK	26	19	I/O	Shift clock. The SCLK signal clocks serial data in through DIN and out through DOUT during the frame-sync interval. When configured as an output (M/$\overline{S}$ high), SCLK is generated internally by multiplying the frame-sync signal frequency by 256. When configured as an input (M/$\overline{S}$ low), SCLK is generated externally and must be synchronous with the master clock and frame sync.

NOTES: 1. Separate analog and digital power and ground pins are supplied on this device. For best operation and results, the PC board designer should utilize separate analog and digital power supplies as well as separate analog and digital ground planes.
2. All digital inputs and outputs are TTL compatible, unless otherwise noted (for DV_{DD} = 5 V).

1.6 Definitions and Terminology

ADC Channel	The ADC channel refers to all signal processing circuits between the analog input and the digital conversion results at DOUT.
Channel Delay	The delay for the analog signal at the ADC input to appear on the digital output. The delay for the digital value at the DAC input to appear on the analog output.
d	The alpha character *d* represents valid programmed or default data in the control register format (see Section 3.2) when discussing other data bit portions of the register.
Dxx	Dxx is the bit position in the primary data word (xx is the bit number).
DSxx	DSxx is the bit position in the secondary data word (xx is the bit number).
DAC Channel	DAC channel refers to all signal processing circuits between the digital data word applied to DIN and the differential output analog signal available at OUTP and OUTM.
Data Transfer Interval	The time during which data is transferred from DOUT and to DIN. The interval is 16 shift clocks and the data transfer is initiated by the falling edge of the frame-sync signal.
FIR	Finite duration impulse response
f_S	The sampling frequency
Frame Sync and Sampling Period	Frame sync and sampling period is the time between falling edges of successive primary frame-sync signals. It is always equal to 256 SCLK.
Frame Sync	Frame sync refers only to the falling edge of the signal that initiates the data transfer interval. The primary frame sync starts the primary communications, and the secondary frame sync starts the secondary communications.
Frame-Sync Interval	The frame-sync interval is the time period occupied by 16 shift clocks. The frame-sync signal goes high on the seventeenth rising edge of SCLK.
Host	A host is any processing system that interfaces to DIN, DOUT, SCLK, $\overline{\text{FS}}$, and/or MCLK.
PGA	Programmable gain amplifier
Primary Communications	Primary communications refers to the digital data transfer interval. Since the device is synchronous, the signal data words from the ADC channel and to the DAC channel occur simultaneously.
Secondary Communications	Secondary communications refers to the digital control and configuration data transfer interval into DIN and the register read data cycle from DOUT. The data transfer interval occurs when requested by hardware or software.
Signal Data	This refers to the input signal and all of the converted representations through the ADC channel and the signal through the DAC channel to the analog output. This is contrasted with the purely digital software control data.
X	The alpha character *X* represents a *don't care* bit-position within the control register format.

1.7 Register Functional Summary

There are seven control registers that are used as follows:

Register 0 The No-Op register. Addressing register 0 allows secondary communications requests without altering any other register.

Register 1 Control register 1. The data in this register controls:

- Software reset
- Software power down
- Normal or auxiliary analog inputs enabling
- Normal or auxiliary analog inputs monitoring
- Selection of monitor amplifier output gain
- Selection of digital loopback
- Selection of16-bit or (15+1)-bit mode of DAC operation

Register 2 Control register 2. The data in this register:

- Contains the output value of FLAG
- Selects phone mode
- Contains the output flag indicating a decimator FIR filter overflow
- Selects either 16-bit mode or (15+1)-bit mode of ADC operation
- Enables analog loopback

Register 3 Control register 3. The data in this register:

- Sets the number of SCLK delays between $\overline{FS}$ and $\overline{FSD}$
- Informs the master device of how many slaves are connected in the chain

Register 4 Control register 4. The data in this register:

- Selects the amplifier gain for the input and output amplifiers
- Sets the sample rate by choosing the value of *N* from 1 to 8 where f_S = MCLK/(128 $\times$ *N*) or MCLK/(512 $\times$ *N*)
- Selects the PLL. If the PLL is selected, the sampling rate is set to MCLK/(128 $\times$ *N*). If the PLL is bypassed, the sampling rate can be set to MCLK/(512 $\times$ *N*).

Register 5 Reserved for factory test. Do not write to this register.

Register 6 Reserved for factory test. Do not write to this register.

2 Detailed Description

2.1 Device Functions

2.1.1 Operating Frequencies and Filter Control

The sampling frequency is controlled by control register 4. When the internal PLL is enabled (D7=0), the sampling frequency is derived from the following equation:

$$f_S = \text{Sampling (conversion) frequency} = \frac{\text{MCLK}}{128 \times N} \quad (1)$$

When the internal PLL is disabled (D7=1), the sampling frequency is derived from the following equation:

$$f_S = \text{Sampling (conversion) frequency} = \frac{\text{MCLK}}{512 \times N} \quad (2)$$

If the sampling frequency is lower than 7 kHz, the sampling frequency is derived from the master clock (MCLK) using equation 2. The internal PLL must be bypassed. The PLL input clock for sampling frequencies lower than 7 kHz is outside the working range for the PLL input clock.

The frequency of SCLK is derived from sampling frequency (fs) instead of MCLK. The equation is as follows:

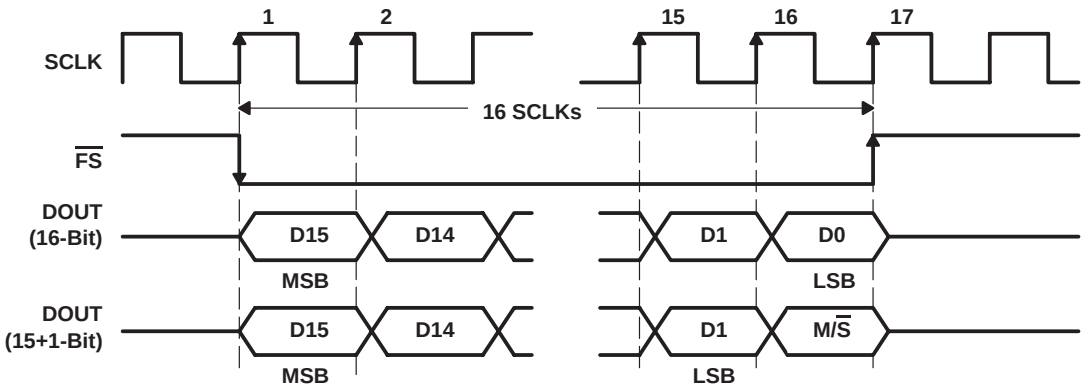
$$\text{SCLK} = 256 \times f_S \quad (3)$$

The cutoff frequency of the filter can not be controlled by register programming. The filter response is shown in the specification for an 8 kHz sample rate. This pass band scales linearly with the sample rate.

2.1.2 ADC Signal Channel

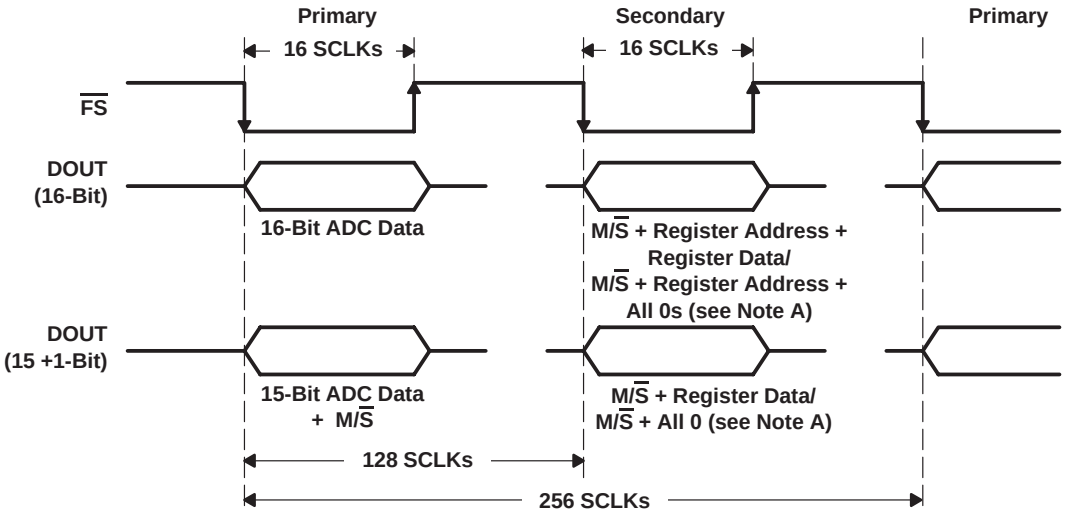
The input signal is amplified and applied to the ADC input. The ADC converts the signal into discrete output digital words in 2s-complement data format, corresponding to the instantaneous analog-signal value at the sampling time. These 16-bit (or 15-bit) digital words, representing sampled values of the analog input signal after the PGA, are clocked out of the serial port (DOUT) at the positive edge of SCLK during the frame-sync interval, one bit for each SCLK and one word for each primary communication interval (256 SCLKs). The 16-bit or (15 + 1)-bit ADC mode is programmed into the device using control register 2. The default setting is the (15 + 1)-bit mode after power-up.

During secondary communication, the data previously programmed into the registers can be read out. This read operation is accomplished by sending the appropriate register address (DS12 – DS8) with the read bit (DS13) set to 1 in through DIN during present secondary communication. If a register read is not requested, all 16 bits are cleared to 0 in the secondary communication. The timing sequence is shown in Figure 2–1 and Figure 2–2.



NOTES: A. The 16-bit or (15 + 1)-bit mode is programmed via control register 2.
B. M/$\overline{S}$ is used to indicate whether the 15-bit data comes from master device or slave device. (Master: M/$\overline{S}$ = 1, Slave M/$\overline{S}$ = 0)
C. The MSB (D15) is stable (the host can latch the data in at this time) at the falling edge of SCLK #1, the last bit (D0,M/$\overline{S}$) is stable at the falling edge of SCLK #16.

Figure 2–1. Timing Sequence of ADC Channel (Primary Communication Only)

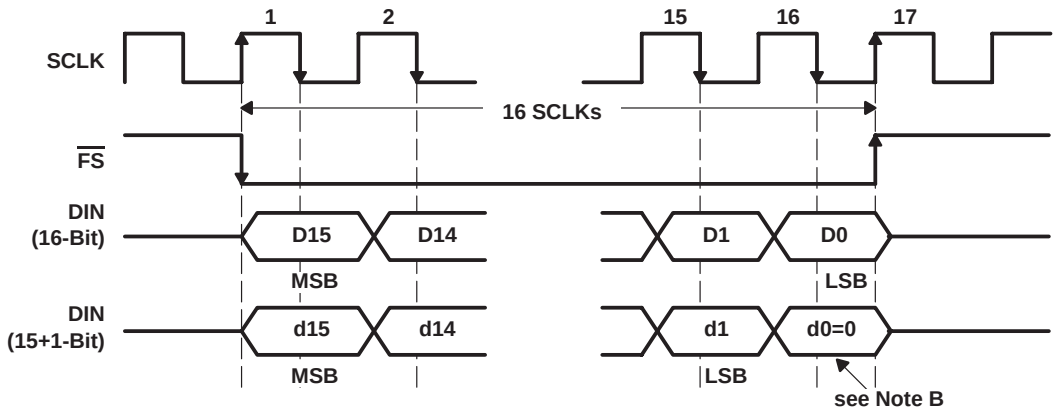


NOTE A: M/$\overline{S}$ bit (DS15) in the secondary communication is used to indicate whether the register data (address and content) comes from the master device or the slave device if the read bit is set. During register read operations, bits DS7 – DS0 are the contents of the specified register. In register write operations, bits DS7 – DS0 are all 0s.

Figure 2–2. Timing Sequence of ADC Channel (Primary and Secondary Communication)

2.1.3 DAC Signal Channel

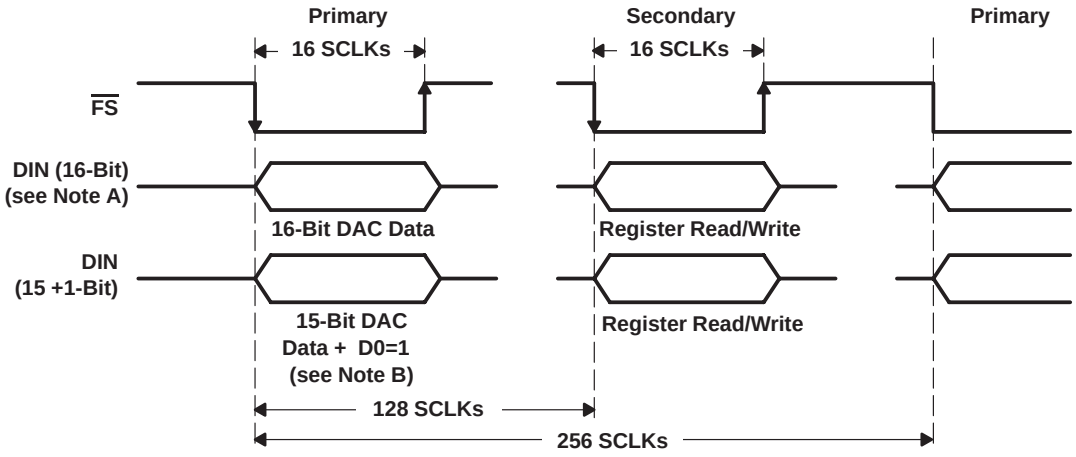
DIN receives the 16-bit serial data word (2s complement) from the host during the primary communications interval. These 16-bit digital words, representing the analog output signal before PGA, are clocked into the serial port (DIN) at the falling edge of SCLK during the frame-sync interval, one bit for each SCLK and one word for each primary communication interval (256 SCLKs). The data are converted to a pulse train by the sigma-delta DAC, which consists of a digital interpolation filter and a digital modulator. The output of the modulator is then passed to an internal low-pass filter to complete the analog signal reconstruction. Finally, the resulting analog signal is applied to the input of a programmable-gain amplifier, which is capable of driving a 600-Ω load differentially at OUTP and OUTM. The timing sequence is shown in Figure 2–3.



NOTES: A. The 16-bit or (15 + 1)-bit mode is programmed via control register 1.
B. d0 = 0 means no secondary communication request (software secondary communication request control—paragraph 3.2)

Figure 2–3. Timing Sequence of DAC Channel (Primary Communication Only)

During secondary communication, the digital control and configuration data (together with the register address), are clocked in through DIN. These 16-bits of data are used either to initialize the register, or to read the register content through DOUT. If a register initialization is not required, a no-operation word (DS15–DS8 are all set to 0) can be used. If DS13 is set to 1, the content of the control register, specified by DS12–DS8, will be sent out through DOUT during the same secondary communication (see section 2.1.5). The timing sequence is shown in Figure 2–4.



NOTES: A. FC has to be set high for a secondary communication request when 16–bit DAC data format is used (paragraph 3.2).
B. D0 = 1 means secondary communication request (software secondary communication request control—paragraph 3.2).

Figure 2–4. Timing Sequence of DAC Channel (Primary and Secondary Communication)

2.1.4 Serial Interface

The digital serial interface consists of the shift clock (SCLK), the frame-sync signal ($\overline{FS}$), the ADC-channel data output (DOUT), and the DAC-channel data input (DIN). During the primary frame synchronization interval, SCLK clocks the ADC channel results out through DOUT and clocks 16-bit/(15+1)-bit DAC data in through DIN.

During the secondary frame-sync interval, SCLK clocks the register read data out through DOUT if the read bit (DS13) is set to 1 and transfers control and device parameter in through DIN. The timing sequence is shown in Figures 2–2 and 2–4.

2.1.5 Register Programming

All register programming occurs during secondary communications through DIN, and data is latched and valid on the falling edge of SCLK during the frame-sync signal. If the default value for a particular register is desired, that register

does not need to be addressed during the secondary communications interval. The no-op command (DS15–DS8 all set to 0) addresses the pseudoregister (register 0), and no register programming takes place during the communications.

In addition, each register can be read back through DOUT during secondary communications by setting the read bit (DS13) to 1. When the register is in the read mode, no data can be written to the register during this cycle. DS13 must be cleared to write to the register.

For example, if the contents of control register 1 is desired to be read out from DOUT, the following procedure must be performed through DIN:

1. Request secondary communication by setting either D0 = 1 (software request) or FC = high (hardware request) during the primary communication interval.
2. At the secondary communication interval ($\overline{FS}$), send data in the following format in through DIN:

		read	control register 1													
0	0	1	0	0	0	0	1	x	x	x	x	x	x	x	x

DS15 DS0

3. Then the following data will be read from DOUT, the last 8 bits of DOUT will contain the register 1 data.

		read	control register 1					data							
M/$\overline{S}$	0	1	0	0	0	0	1	d	d	d	d	d	d	d	d

DS15 DS0

Figure 2–5 is a timing diagram of this procedure.

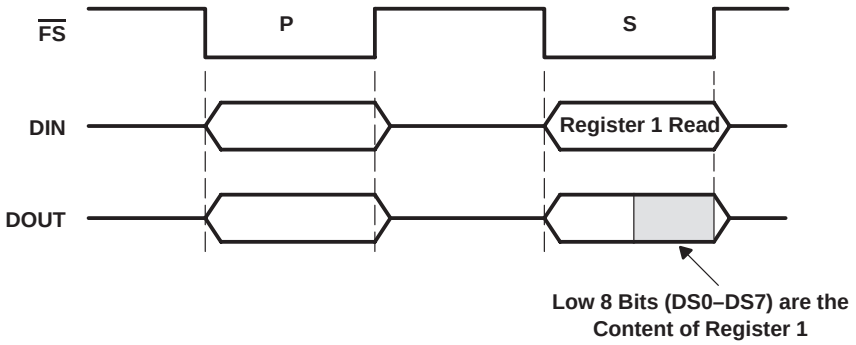


Figure 2–5. Register 1 Read Operation Timing Diagram

If control register 1 needs to be programmed, the following procedure must be performed through DIN:

1. Request secondary communication by setting either D0 = 1 (software request) or FC = high (hardware request) during the primary communication interval.
2. At the secondary communication interval ($\overline{FS}$), send data in the following format in through DIN:

		write	control register 1					data							
0	0	0	0	0	0	0	1	d	d	d	d	d	d	d	d

DS15 DS0

3. Then the following data is generated from DOUT:

		write	control register 1												
M/$\overline{S}$	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

DS15 DS0

Figure 2–6 is a timing diagram of this procedure.

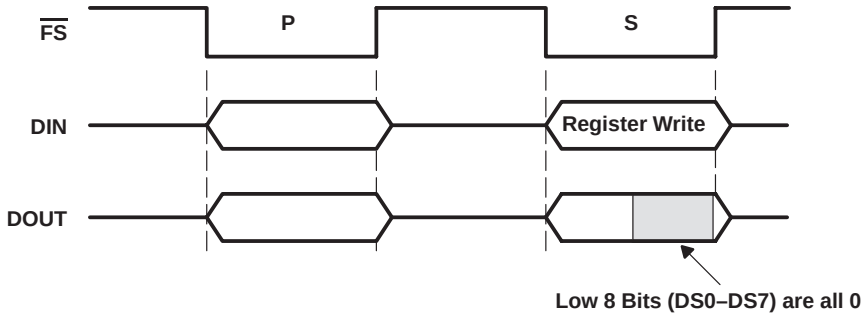


Figure 2–6. Register 1 Write Operation Timing Diagram

2.1.6 Sigma-Delta ADC

The sigma-delta analog-to-digital converter in the device is a sigma-delta modulator with 64-× oversampling. The ADC provides high-resolution, low-noise performance using oversampling techniques. Due to the oversampling employed, only single-pole antialiasing filters are required on the analog inputs.

2.1.7 Decimation Filter

The decimation filters reduce the digital data rate to the sampling rate. This is accomplished by decimating with a ratio of 1:64. The output of the decimation filter is a 16-bit 2s-complement data word clocking at the sample rate selected for that particular data channel. The bandwidth of the filter is $0.439 \times f_{sample}$ and scales linearly with the sample rate.

2.1.8 Sigma-Delta DAC

The sigma-delta digital-to-analog converter in the device is a sigma-delta modulator with 256-× oversampling. The DAC provides high-resolution, low-noise performance using oversampling techniques.

2.1.9 Interpolation Filter

The interpolation filter resamples the digital data at a rate of 256 times the incoming sample rate. The high-speed data output from the interpolation filter is then used in the sigma-delta DAC. The bandwidth of the filter is $0.439 \times f_{sample}$ and scales linearly with the sample rate.

2.1.10 Analog and Digital Loopback

The analog and digital loopbacks provide a means of testing the modem data ADC/DAC channels and can be used for in-circuit system-level tests. The analog loopback routes the DAC low-pass filter output into the analog input where it is then converted by the ADC into a digital word. The digital loopback, enabled by setting bit D1 in control 1 register to 1, routes the ADC output to the DAC input on the device. Analog loopback is enabled by setting bit D3 in control 2 register to 1 (see section 6).

2.1.11 FIR Overflow Flag

The decimator FIR filter sets an overflow flag (bit D5) of control 2 register to indicate that the input analog signal has exceeded the range of the internal decimation filter calculations. Once the FIR overflow flag has been set in the register, it remains set until the register is read by the user. Reading this value resets the overflow flag.

If FIR overflow occurs, the input signal must be attenuated either by the PGA or some other method.

2.2 Reset and Power-Down Functions

2.2.1 Software and Hardware Reset

The TLC320AD50C and TLC320AD52C reset the internal counters and registers in response to either of two events:

1. A low-going reset pulse is applied to terminal $\overline{\text{RESET}}$.
2. A 1 is written to the programmable software reset bit (D7 of control register 1).

Either event resets the control registers and clears all the sequential circuits in the device. Reset signals should be at least 6 master clock periods long.

After hardware reset, the default contents of all registers is 0.

After a hardware or software reset, the AD50 and AD52 require a finite amount of time for the internal PLL to stabilize. During this time, no control words or D/A data should be written to the device.

The reset sequence should be as follows:

1. Assert reset (pulse width encompassing at least 6 MCLK periods)
2. Deactivate reset
3. Wait for SCLKS to be generated by the master device. This will take approximately 100 μs.
4. Wait for 18 frame syncs to occur
5. Write control and configuration data
6. Collect conversion data

2.2.2 Software and Hardware Power Down

Except for the digital interface, most of the device enters the power-down mode when D6 in control 1 register is set to 1. When $\overline{\text{PWRDWN}}$ is taken low, the entire device is powered down. In either case, the register contents are preserved and the output of the monitor amplifier is held at the midpoint voltage to minimize pops and clicks.

The amount of power drawn during software power down is higher than it is during a hardware power down because of the current required to keep the digital interface active. Additional differences between software and hardware power-down modes are detailed in the following paragraphs. Figure 2–7 represents the internal power-down logic.

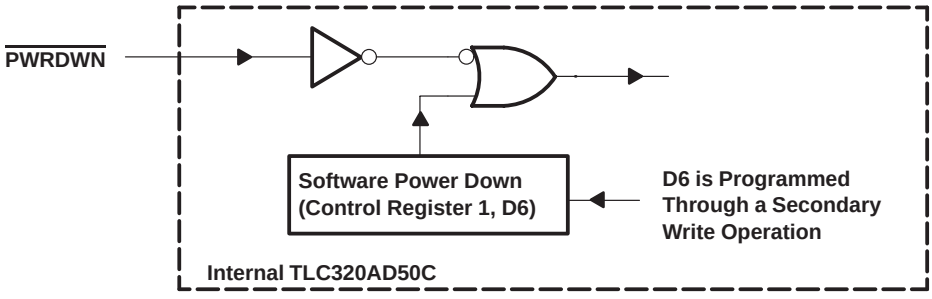


Figure 2–7. Internal Power-Down Logic

2.2.2.1 Software Power Down

When D6 of control 1 register is set to 1, the device enters the software power-down mode. In this state, the digital interface circuit is still active while the internal ADC and DAC channels and differential outputs OUTP and OUTM are disabled, and DOUT and $\overline{\text{FSD}}$ are inactive. Register data in the secondary serial communications is still accepted, but data in the primary serial communications is ignored. The device returns to normal operation when D6 of control 1 register is reset to 0.

2.2.2.2 Hardware Power Down

When $\overline{\text{PWRDWN}}$ is held low, the device enters the hardware power-down mode. In this state, the internal clock control circuit and the differential outputs OUTP and OUTM are disabled. All other digital I/Os either are disabled or remain in the state they were in immediately before power down. DIN cannot accept any data input. The device can only be returned to normal operation by taking and holding $\overline{\text{PWRDWN}}$ high. When not holding the device in the hardware power-down mode, $\overline{\text{PWRDWN}}$ should be tied high.

2.3 Master Clock Circuit

MCLK is the external master clock input. The internal clock circuit generates and distributes necessary clocks throughout the device. An internal PLL circuit is used for upsampling to provide the appropriate clocks for the digital filters and modulators.

When the device is in the master mode, SCLK and $\overline{\text{FS}}$ are derived from MCLK in order to provide clocking of the serial communications between the device and its controller. When in the slave mode, SCLK and $\overline{\text{FS}}$ are both inputs.

2.4 Data Out (DOUT)

DOUT is placed in the high-impedance state on the rising edge of the frame sync. In the primary communication, the data word is the ADC conversion result. In the secondary communication, the data is the register-read results when requested by the read/write (R/$\overline{\text{W}}$) bit. If a register read is not requested, the low eight bits of the secondary word are all zeroes. The state of the master/slave (M/$\overline{\text{S}}$) terminal is reflected by the MSB in secondary communication (DOUT, bit DS15) and the LSB in the primary communication (DOUT, bit D0) while in 15 + 1 mode. When the device is in the slave mode, DOUT remains in a high-impedance state until a nonzero value is written as a number of slaves in control register 3 (bits D7 and D6).

2.4.1 Data Out, Master Mode

In the master mode, DOUT is taken from the high-impedance state by the falling edge of the frame sync ($\overline{\text{FS}}$) that is assigned to DOUT. The most significant data bit then appears first on DOUT.

2.4.2 Data Out, Slave Mode

In the slave mode, DOUT is taken from the high-impedance state by the falling edge of the input frame sync ($\overline{\text{FS}}$). The most significant data bit then appears on DOUT. When in the slave mode, DOUT is not enabled until the control 3 register is programmed with the number of slaves. This must be done even if there is only one slave device.

2.5 Data In (DIN)

In a primary communication, the data word is the input digital signal to the DAC channel. If the (15+1)-bit data format is used, the LSB (D0) is used to request a secondary communication. In a secondary communication, the data is the control and configuration data that sets the device for a particular function (see Section 3, Secondary Serial Communication for details).

2.6 FC (Hardware Secondary Communication Request)

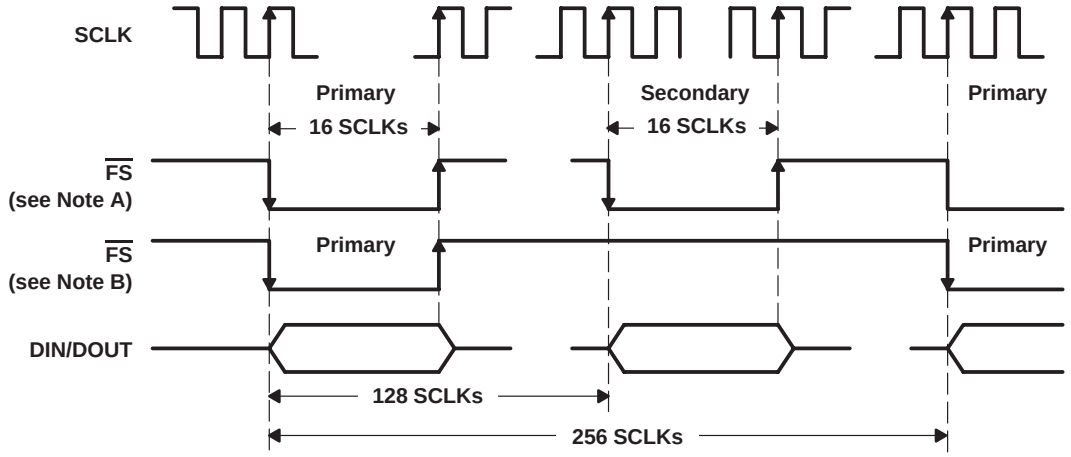
The FC input provides for hardware requests for secondary communications. FC works in conjunction with the LSB of the primary data word. The signal on FC is latched on the rising edge of the primary frame sync ($\overline{\text{FS}}$). FC should be tied low if not used.

2.7 Frame-Sync Function for TLC320AD50C

The frame-sync signal ($\overline{\text{FS}}$) indicates the device is ready to send and receive data. The data transfer out of DOUT and into DIN begins on the falling edge of the frame-sync signal.

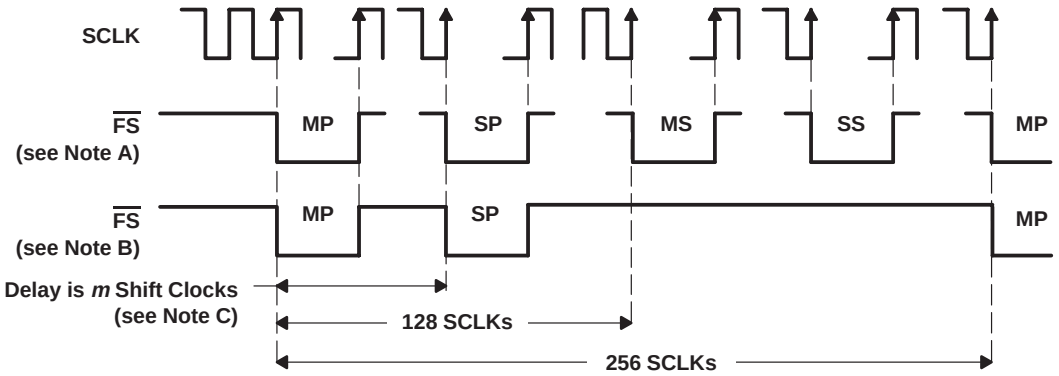
2.7.1 Frame Sync ($\overline{FS}$) Function, Master Mode

The frame sync is generated internally and goes low on the rising edge of SCLK and remains low during a 16-bit data transfer. In addition to generating its own frame-sync signal, the master also outputs a frame sync for each slave that is being used (see Figures 2–8 and 2–9).



NOTES: A. Primary and secondary serial communication
B. Primary serial communication, only

Figure 2–8. Master Device Frame-Sync Signal With Primary and Secondary Communications (No Slaves)



Legend:
MP: Master Primary (master device data is transferred in this period, DOUT of the slave device is in high impedance state).
SP: Slave Primary (slave device data is transferred in this period, DOUT of master device is in high impedance state).
MS: Master Secondary (master device control register information is transferred in this period, DOUT of the slave device is in high impedance state).
SS: Slave Secondary(slave device control register information is transferred in this period, DOUT of the master device is in high impedance state).

NOTES: A. Primary and secondary serial communications
B. Primary serial communication only
C. *m* is the value programmed into the FSD register (control register 3: D0–D5)

Figure 2–9. Master Device Frame-Sync Signal With Primary and Secondary Communications (With 1 Slave Device)

2.7.2 Frame Sync ($\overline{FS}$) Function,Slave Mode

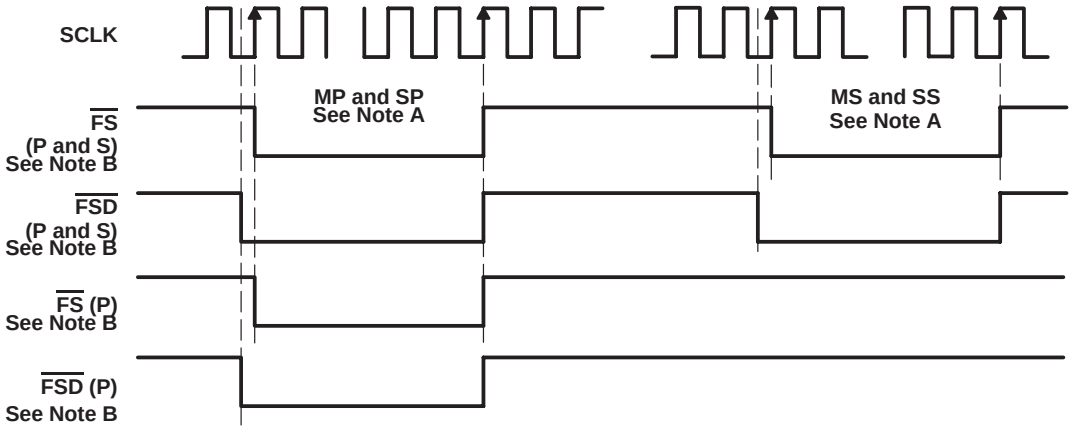
Frame-sync timing is generated externally by the master $\overline{FSD}$ (or the previous slave in a multislave configuration) and is applied to $\overline{FS}$ of the slave to control the ADC and DAC timing.

2.7.3 Frame-Sync Delayed ($\overline{\text{FSD}}$) Function, Master Mode

The timing relationships are as follows:

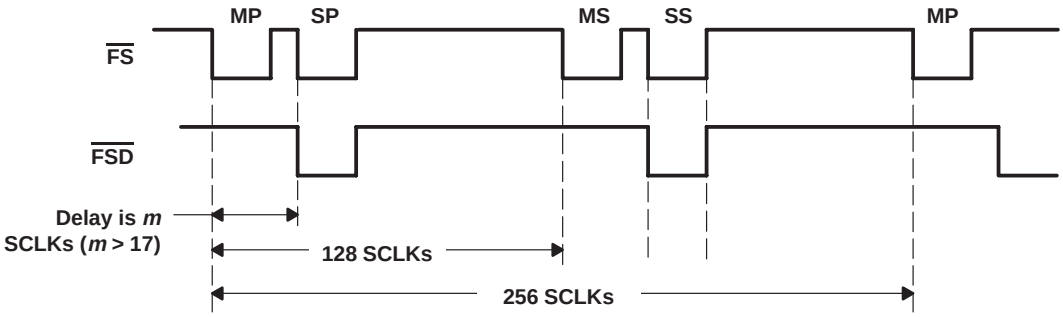
- When the FSD register (control 3 register) data is 0 (default state at power up), then $\overline{\text{FSD}}$ goes low 1/4 SCLK prior to the rising edge of SCLK when $\overline{\text{FS}}$ goes low (Figure 2–10).
- When the FSD register data is greater than 17, then $\overline{\text{FSD}}$ goes low on the rising edge of SCLK that is the $\overline{\text{FSD}}$ register number of SCLKs after the falling edge of $\overline{\text{FS}}$ (Figure 2–11).

Register data values from 1 to 17 result in a default register value of zero and should not be used.



NOTES: A. The DIN of master and slave devices share the same DIN bus during first initialization. The DOUT is occupied by the master device only until the control 3 register of master and slave device is programmed with slave devices number and number of SCLKs between FS and FSD (m>17).
B. P&S: Primary and secondary communications P: Primary communication only

Figure 2–10. Master Device $\overline{\text{FS}}$ and $\overline{\text{FSD}}$ Output When $\overline{\text{FSD}}$ Register (D0–D5, Control 3 Register) is 0



NOTES: A. Since master and slave share the same DIN bus during first initialization, they share the same input data word. Only one write cycle is needed to program control 3 register of master device and slave device(s).
B. After the control 3 register is programmed, the DIN or DOUT bus of master and slave(s) are separated by time, although they still physically connect to each other.

Figure 2–11. Master Device $\overline{\text{FS}}$ and $\overline{\text{FSD}}$ Output After Control 3 Register Is Programmed (One Slave Device)

2.7.4 Frame-Sync Delayed ($\overline{\text{FSD}}$), Slave Mode

The master $\overline{\text{FSD}}$ is output to the first slave device and the first slave $\overline{\text{FSD}}$ is output to the second slave device and so on (see Figure 2–12). The $\overline{\text{FSD}}$ output of each device is input to the $\overline{\text{FS}}$ terminal of the succeeding device. The $\overline{\text{FSD}}$ timing sequence in the slave mode is as follows:

- When the FSD register data is 0, then $\overline{\text{FSD}}$ goes low 1/4 SCLK cycle before $\overline{\text{FS}}$ goes low.
- When the FSD register data is greater than 17, then $\overline{\text{FSD}}$ goes low on the rising edge of the SCLK that is equal to the FSD register number of SCLKs after the falling edge of $\overline{\text{FS}}$ (see Figure 2–13).

Data values from 1 to 17 should not be used.

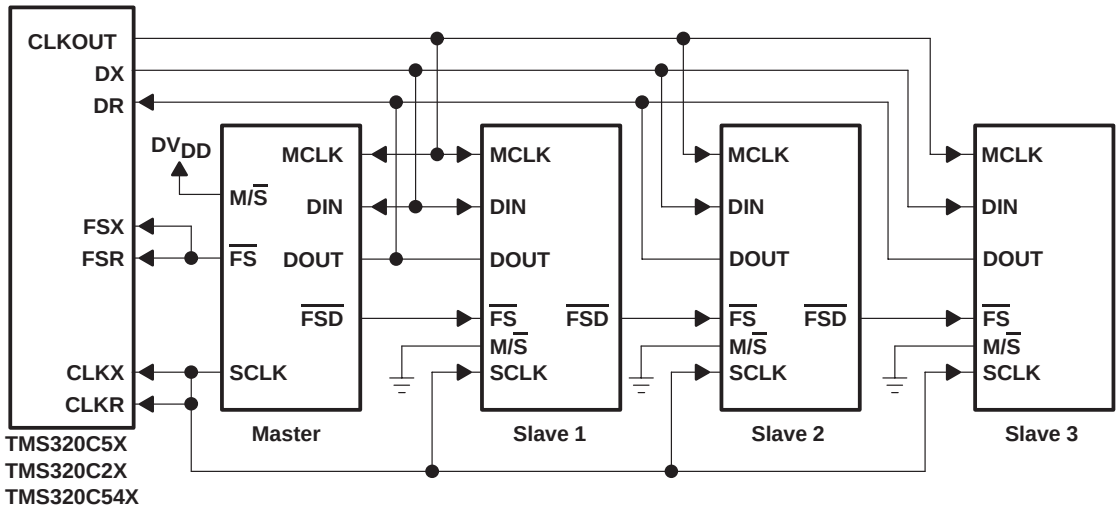
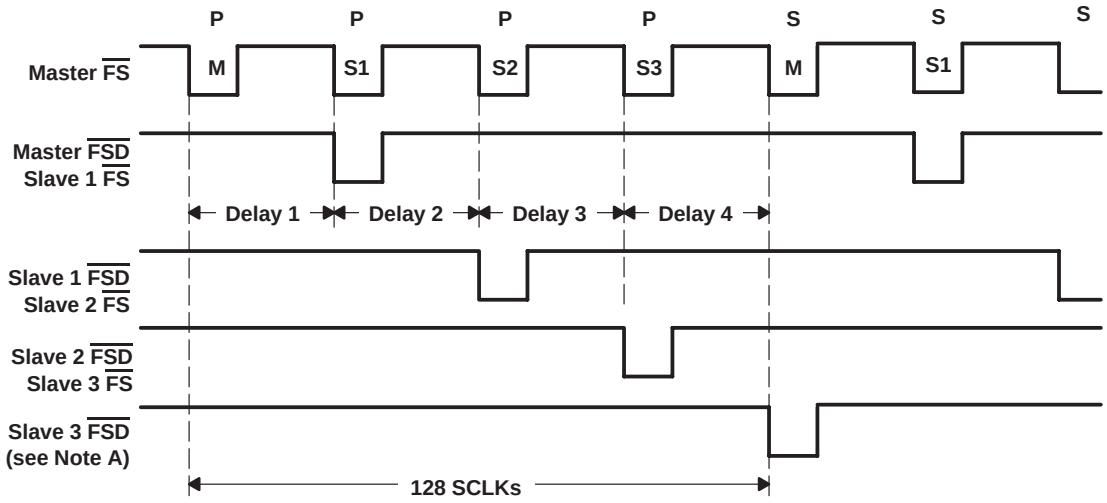


Figure 2–12. Master With Slaves (To DSP Interface)



NOTE A: Slave 3 FSD cannot be used.

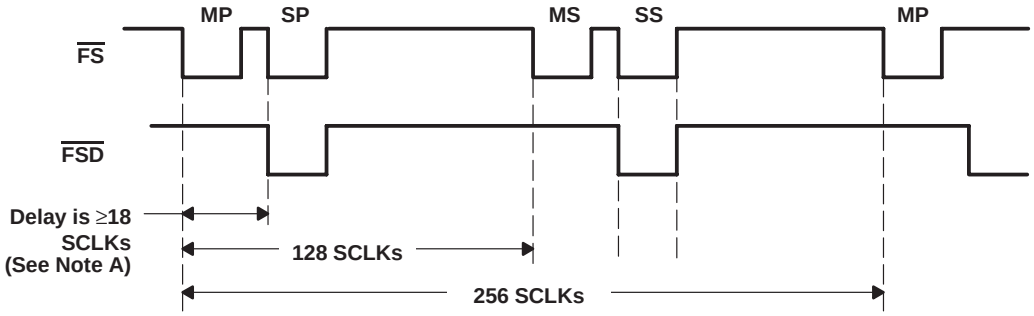
Figure 2–13. Master-Slave Frame-Sync Timing After A Delay Has Been Programmed Into The FSD Register (D0–D5 of Control 3 Register)

2.8 Frame-Sync Function for TLC320AD52C

The frame-sync function for TLC320AD52C is very similar to that of the TLC320AD50C except the following:

1. TLC320AD52C can support only one slave.
2. The $\overline{\text{FSD}}$ terminal function can be disabled for TLC320AD52C by programming bit D2 in control 2 register.
3. The $\overline{\text{FSD}}$ value loaded into control 3 register must be multiplied by 2 to obtain the actual number of SCLKs for the delay.

For example, if $\overline{\text{FSD}}$ register (control register 3) is programmed with 49H, it means that the TLC320AD52C has one slave and the $\overline{\text{FSD}}$ terminal has 18 SCLKs delay after master primary $\overline{\text{FS}}$ output. See Figure 2–14.

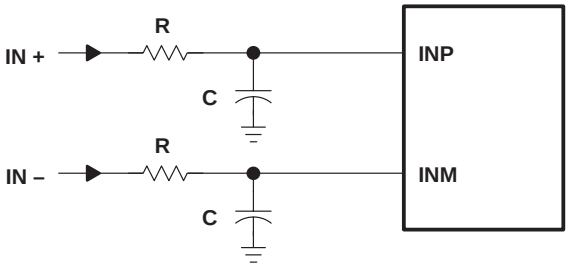


NOTE A: Minimum SCLK delay number in $\overline{\text{FSD}}$ register is 9. This means that a delay of at least 18 SCLKs is required for proper operation of the TLC320AD52C.

Figure 2–14. Master Device $\overline{\text{FS}}$ and $\overline{\text{FSD}}$ Output After Control 3 Register Is Programmed With 49H

2.9 Multiplexed Analog Input and Output

The two differential analog inputs (INP and INM or AUXP and AUXM) are multiplexed into the sigma-delta modulator. The performance of the AUX channel is similar to the normal input channel. A single-pole antialias filter must be connected to INP and INM (also AUXP and AUXM, if used). If an RC is used for the single-pole filter (Figure 2–15) the value of R should not be greater that 1 kΩ. The gain of the input amplifiers is set through the control register 4.



NOTES: A. The bandwidth of this RC antialias is determined by: ($f_0 = 1/(2\pi RC)$)
B. AUXP and AUXM need to be connected to AV_{SS} if not used.
C. Bandwidth of the antialias filter can be $4 \times f_S$.
D. The input signal must have $AV_{DD}/2$ dc or it must be ac-coupled.

Figure 2–15. RC Antialias Filter

To produce the best possible common-mode rejection of unwanted signal performance, the analog signal is processed differentially until it is converted to digital data. The signal applied to the terminals INM and INP should be differential to preserve the device specifications. As much as 6 dB of signal level will be lost if the single-ended input is used directly. The signal source driving the analog inputs (INP and INM or AUXP and AUXM) should have a low source impedance for best low-noise performance and accuracy.

To obtain maximum dynamic range, the signal should be ac-coupled to the input terminal. The analog input signal is self-biased to the midsupply voltage if the monitor-amplifier input source is selected as the same source for the

ADC input. These input sources are selected by bits D4 and D5 of control register 1. The default condition self-biases the input since the register default value selects INP and INM as the source for both the ADC and monitor amplifier input (see Figure 2–16). A simple single-pole antialias filter with low output impedance must be connected to INP and INM (also AUXP and AUXM, if used).

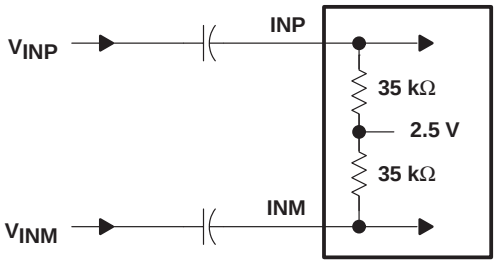


Figure 2–16. INP and INM Internal Self-Biased (2.5 V) Circuit

2.9.1 Analog Output

The OUTP and OUTM are differential outputs and can drive a typical 600-Ω load directly. Figure 2–17 shows the circuit when load is ground referenced.

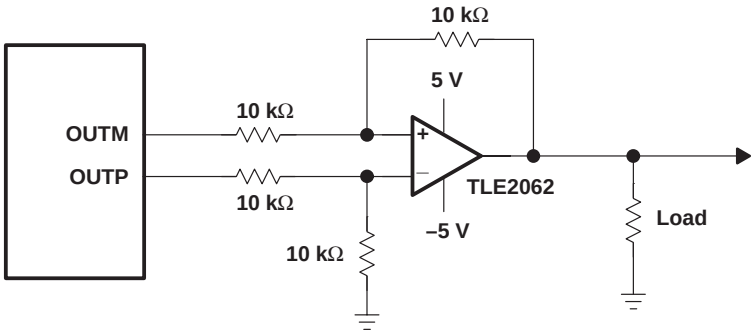
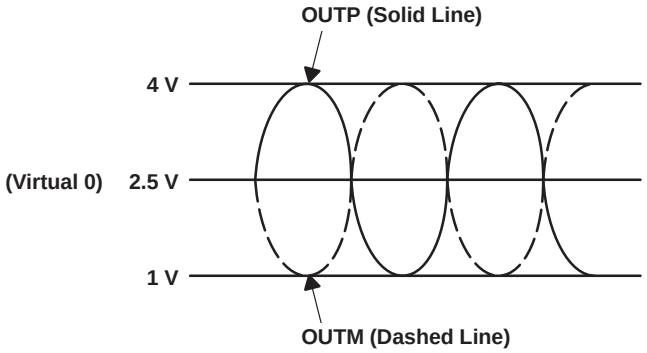


Figure 2–17. Differential Output Drive (Ground Referenced)



	Digital Input Code	Analog Output Voltage OUT +	Analog Output Voltage OUT –
(+FS)	0111 1111 1111 1111	4 V	1 V
(Virtual 0)	0000 0000 0000 0000	2.5 V	2.5 V
(–FS)	1000 0000 0000 0000	1 V	4 V

Figure 2–18. Digital Input Code vs Analog Output Voltage

3 Serial Communications

DOUT, DIN, SCLK, $\overline{FS}$, and FC are the serial communication signals. The digital output data from the ADC is taken from DOUT. The digital input data for the DAC is applied to DIN. The synchronizing clock for the serial communication data and the frame sync is taken from SCLK. The frame-sync pulse that encloses the ADC and DAC data transfer interval is taken from $\overline{FS}$. For signal data transmitted from the ADC or to the DAC, primary serial communication is used. To read or write words that control both the options and the circuit configurations of the device, secondary communication is used.

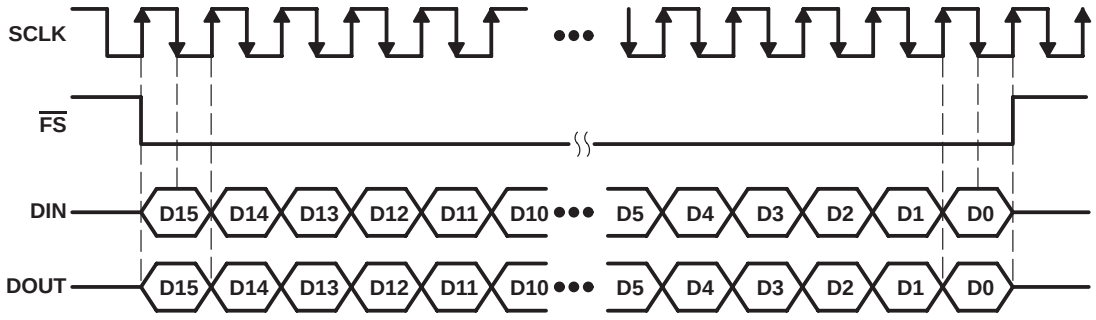
The purpose of the primary and secondary communications is to allow conversion data and control data to be transferred across the same serial port. A primary transfer is always dedicated to conversion data. A secondary transfer is used to set up and/or read the register values. A primary transfer occurs for every conversion period. A secondary transfer occurs only when requested. Secondary serial communication can be requested either by hardware (FC terminal) or by software (D0 of primary data input to DIN).

3.1 Primary Serial Communication

Primary serial communication is used both to transmit and receive conversion signal data. The DAC word length depends on the state of bit D0 in control 1 register. After power up or reset, the device defaults to the 15-bit mode. When the DAC word length is 15 bits, the last bit of the primary 16-bit serial communication word is a control bit used to request secondary serial communication. In the 16-bit mode, all 16 bits of the primary communication word are used as data for the DAC and the hardware terminal FC must be used to request secondary communication.

Figure 3–1 shows the timing relationship for SCLK, $\overline{FS}$, DOUT, and DIN in a primary communication. The timing sequence for this operation is as follows:

1. $\overline{FS}$ is brought low by the TLC320AD50C, TLC320AD50I, or TLC320AD52C.
2. A 16-bit word is transmitted from the ADC (DOUT) and a 16-bit word is received from the DAC (DIN).
3. $\overline{FS}$ is brought high by the TLC320AD50C, TLC320AD50I, or TLC320AD52C, signaling the end of the data transfer.



NOTE: DIN is latched at the falling edge of SCLK. DOUT is sent out at the rising edge of SCLK

Figure 3–1. Primary Serial Communication Timing

3.2 Secondary Serial Communication

Secondary serial communication is used to read or write 16-bit words that program both the options and the circuit configurations of the device. Register programming always occurs during secondary communication. Four primary and secondary communication cycles are required to program the four registers. If the default value for a particular register is desired, then the register addressing can be omitted during secondary communications. The NOOP command addresses a pseudoregister, register 0, and no register programming takes place during this secondary communication. If secondary communication is desired for any device (either master or slave), then a secondary communication must be requested for all devices, starting with the master. This results in a secondary frame sync ($\overline{FS}$) for all devices. The NOOP command can be used for devices that do not need a secondary operation.

During secondary communication, a register may be written to or read from. When writing a value to a register, DIN contains the value to be written. When reading the value in a register, the data is stepped out on DOUT.

There are two methods for initiating secondary communications:

1. By asserting a high level on FC
2. By asserting the LSB of the DIN 16-bit serial communication high while in the15-bit mode

Both methods are illustrated in Figure 3–2.

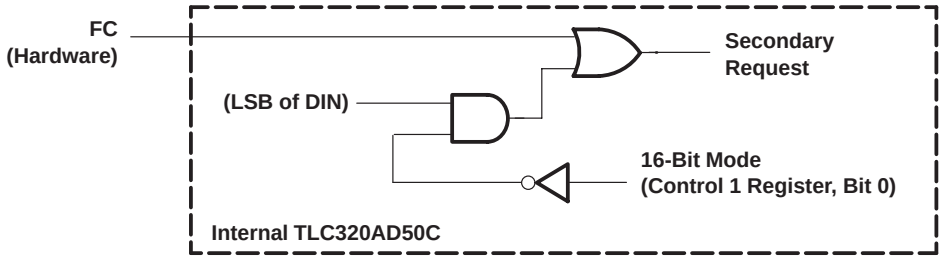


Figure 3–2. Hardware and Software Methods to Make a Secondary Request

FC should be pulled high before the rising edge of the frame sync ($\overline{FS}$). This causes the start of the secondary communication, 128 SCLKs after the start of the primary communication frame. If slaves are present, FC should remain high until the rising edge of the frame sync for the last slave.

The second method for secondary communication is by asserting the LSB high. The least significant bit (D0) can be used for the secondary requests as shown in Table 3–1. The request is made by placing the device in the 15-bit DAC mode and making the LSB of DIN equal to 1. All devices should be in the 15-bit DAC mode and secondary communication should be requested for all devices.

Table 3–1. Least Significant Bit Control Function

CONTROL BIT D0	CONTROL BIT FUNCTION
0	No operation (NOOP)
1	Secondary communication request

If a secondary communication request is made, $\overline{FS}$ goes low after 128 SCLKs after the beginning of the primary frame.

3.2.1 Hardware Secondary Serial Communication Request

The FC requests a secondary communication when it is asserted. The FC terminal is latched at the rising edge of $\overline{FS}$ (primary communication), so FC should be pulled high before the rising edge of the primary frame sync ($\overline{FS}$). Figures 3–3 and 3–4 show the $\overline{FS}$ output from a master device.

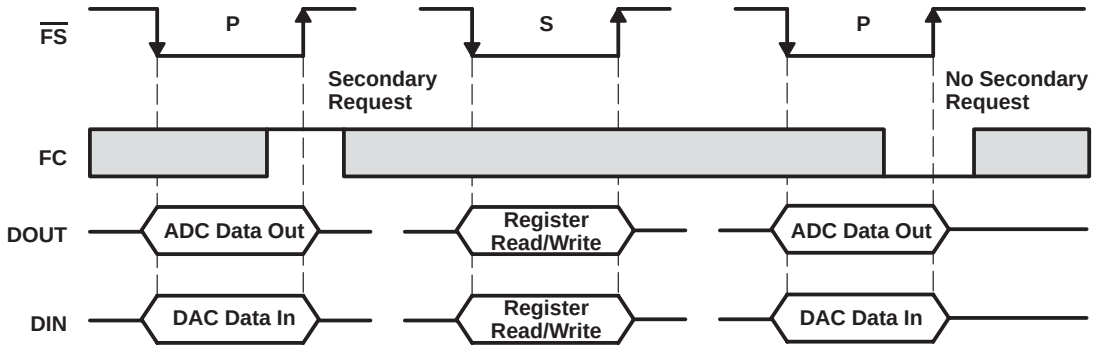
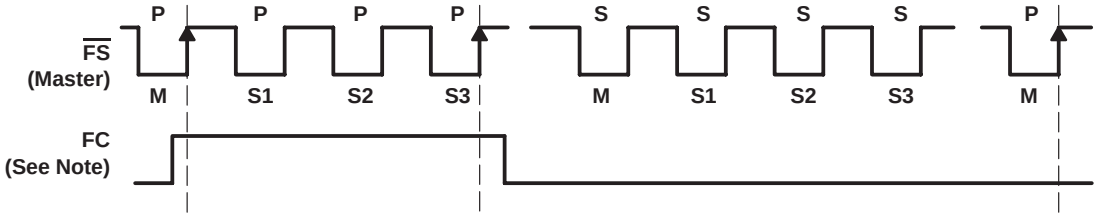


Figure 3–3. $\overline{FS}$ Output When Hardware Secondary Serial Communication Is Requested Only Once (No Slave)



NOTE: FC of master device and slave devices should connect together.

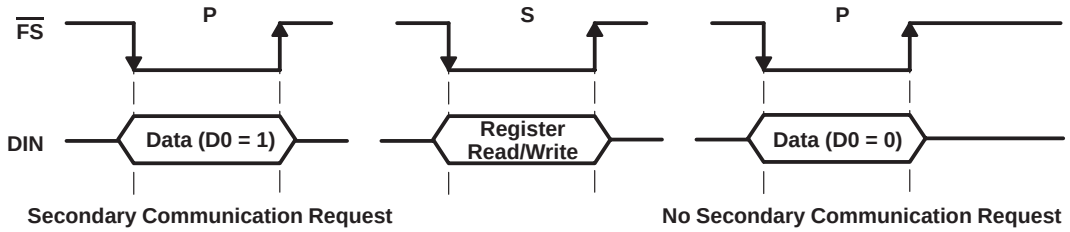
Figure 3–4. $\overline{FS}$ Output When Hardware Secondary Serial Communication Is Requested Only Once (Three Slaves)

3.2.2 Software Secondary Serial Communication Request

The LSB of the DAC data within a primary transfer can request a secondary communication when the device is in the 15-bit mode.

For all serial communications, the most significant bit is transferred first. For a 16-bit ADC word and a 16-bit DAC word, D15 is the most significant bit and D0 is the least significant bit. For a 15-bit DAC data word in a primary communication, D15 is the most significant bit and D1 is the least significant bit. Bit D0 is then used for the secondary communication request control. All digital data values are in 2s complement data format (Figure 3–5).

If the data format is set to the 16-bit word mode, all 16 bits are either ADC or DAC data and secondary communication can then be requested only by hardware (FC terminal).



NOTE: See Figure 3–8 for secondary communication DIN data format.

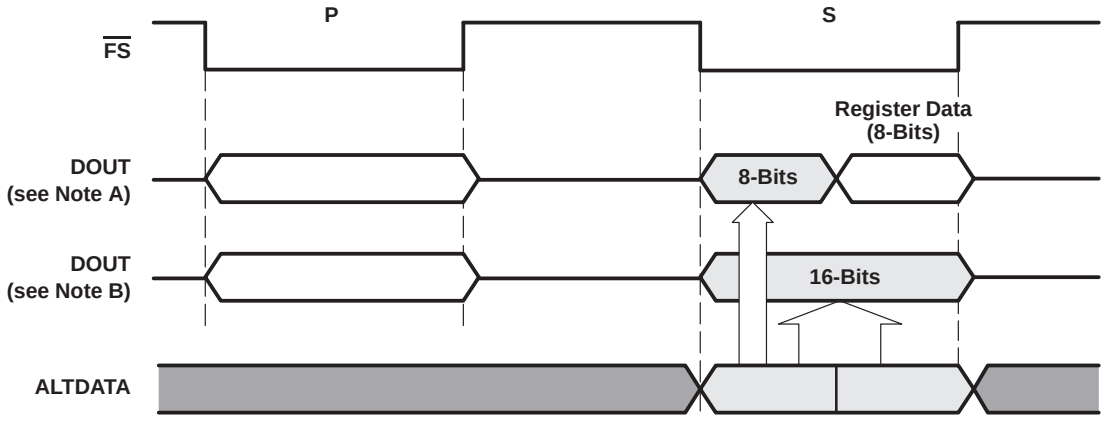
Figure 3–5. $\overline{FS}$ Output During Software Secondary Serial Communication Request (No Slave)

3.3 Conversion Rate Versus Serial Port

The SCLK frequency is set equal to the frequency of the frame-sync signal ($\overline{FS}$) multiplied by 256. The conversion rate or sample rate is equal to the frequency of $\overline{FS}$.

3.4 Phone Mode Control

Phone mode control is provided for applications that need hardware control and monitoring of external events. By allowing the device to drive the FLAG terminal (set through control 2 register), the host DSP is capable of system control through the same serial port that connects the device. Along with this control is the capability of monitoring the value of the ALTDATA terminal during a secondary communication cycle. One application for this function is in monitoring RING DETECT or OFFHOOK DETECT from a phone answering system. FLAG allows response to these incoming control signals. Figure 3–6 shows the timing associated with this operating mode.



NOTES: A. When DIN performs a read operation (set D13 to 1) during secondary communication.
B. When DIN perform a write operation (set D13 to 0) during secondary communication.

Figure 3–6. Phone Mode Timing When Phone Mode Is Enabled

3.5 DIN and DOUT Data Format

3.5.1 Primary Serial Communication DIN and DOUT Data Format (Figure 3–7)

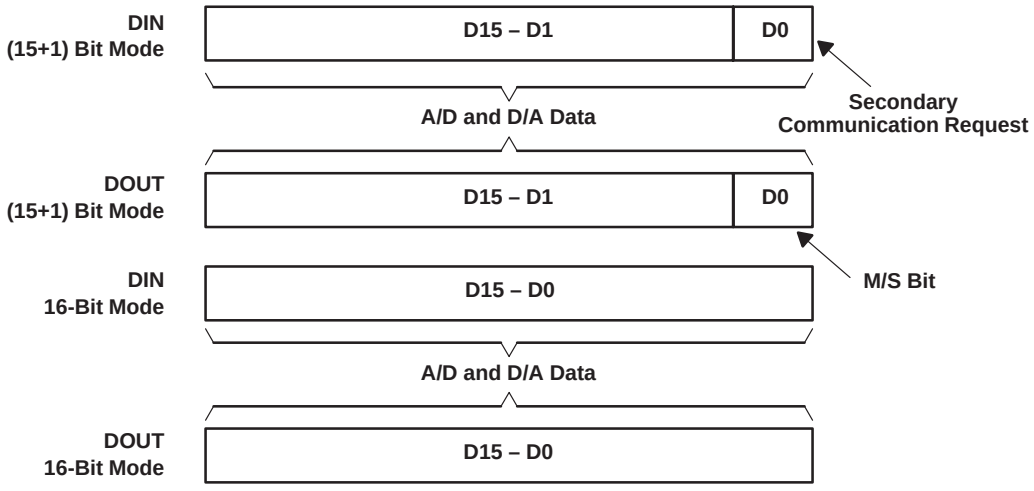


Figure 3–7. Primary Communication DIN and DOUT Data Format

3.5.2 Secondary Serial Communication DIN and DOUT Data Format (Figure 3–8)

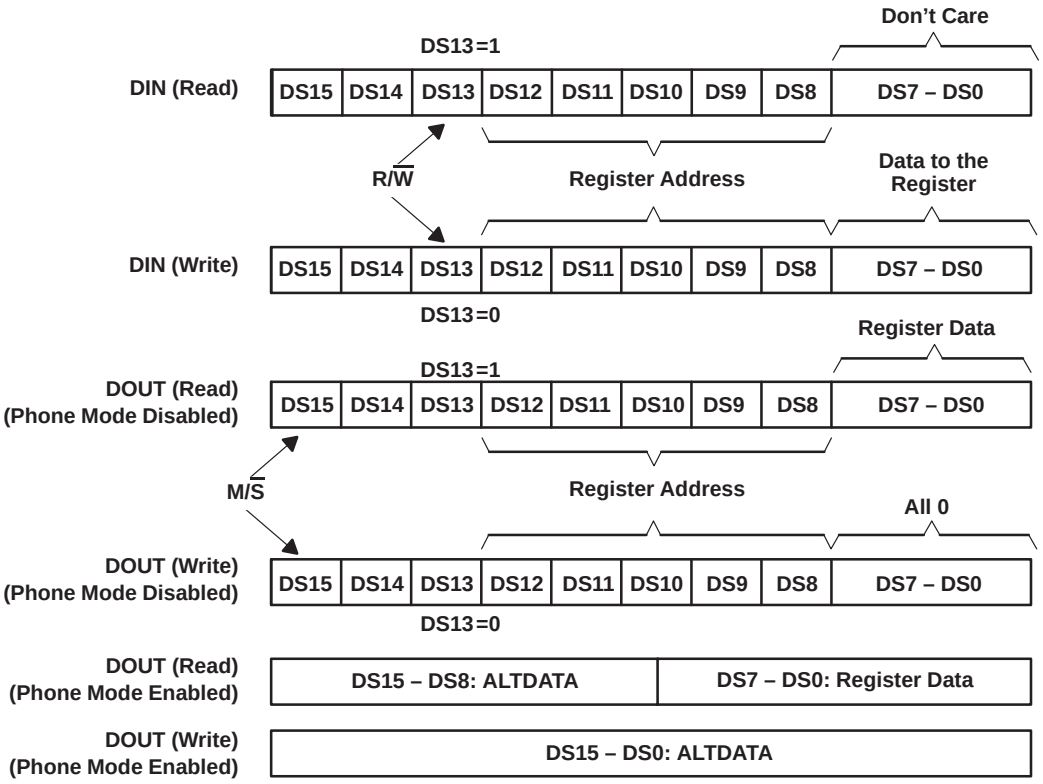


Figure 3–8. Second Communication DIN and DOUT Data Format

4 Specifications

4.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, DV_{DD}, AV_{DD} (see Note 1) . . . . . –0.3 V to 7 V
Output voltage range, DOUT, $\overline{FS}$, SCLK, FLAG . . . . . –0.3 V to DV_{DD} + 0.3 V
Output voltage range, OUTP, OUTM . . . . . –0.3 V to V_{DD} + 0.3 V
Input voltage range, DIN, $\overline{PWRDWN}$, $\overline{RESET}$, ALTDATA, MCLK, FC . . . . . –0.3 V to DV_{DD} + 0.3 V
Input voltage range, INP, INM, AUXP, AUXM . . . . . –0.3 V to V_{DD} + 0.3 V
Case temperature for 10 seconds: DW package . . . . . 260°C
Operating free-air temperature range, TLC320AD50C/52C, T_A . . . . . 0°C to 70°C
Operating free-air temperature range, TLC320AD50I, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

4.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, AV_{DD} (see Note 2)		4.75		5.5	V
Analog signal input voltage, $V_{I(analog)}$	Differential (INP – INM) peak, for full scale operation			6	V
Differential output load resistance, OUTP, OUTM, R_L			600		Ω
Differential output load capacitance, OUTP, OUTM, C_L				15	pF
ADC or DAC conversion rate			8	22.05	kHz
Operating free-air temperature, T_A		0		70	°C

NOTE 2: Voltages at analog inputs and outputs and AV_{DD} are with respect to the AV_{SS} terminal.

4.2.1 Recommended Operating Conditions, DV_{DD} = 5 V

	MIN	NOM	MAX	UNIT
Supply voltage, DV_{DD} (see Note 3)	4.5		5.5	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
MCLK frequency		8.192	11.290	MHz

NOTE 3: Voltages at digital inputs and outputs and DV_{DD} are with respect to the DV_{SS} terminal.

4.2.2 Recommended Operating Conditions, DV_{DD} = 3 V

	MIN	NOM	MAX	UNIT
Supply voltage, DV_{DD} (see Note 3)	2.7	3	3.3	V
High-level input voltage, V_{IH}	1.8			V
Low-level input voltage, V_{IL}			0.6	V
MCLK frequency		8.192	11.290	MHz

NOTE 3: Voltages at digital inputs and outputs and DV_{DD} are with respect to the DV_{SS} terminal.

4.3 Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, DV_{DD} = 5 V, R_L = 600 Ω (Unless Otherwise Noted)

4.3.1 Digital Inputs and Outputs, MCLK = 8.192 MHz, f_S = 8 kHz, DV_{DD} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, DOUT	I_O = 360 µA	4	5		V
V_{OL}	Low-level output voltage, DOUT	I_O = –2 mA		0.2	0.4	V
I_{IH}	High-level input current, any digital input	V_{IH} = 5 V			10	µA
I_{IL}	Low-level input current, any digital input	V_{IL} = 0.8 V			10	µA
C_i	Input capacitance			5		pF
C_o	Output capacitance			5		pF

4.3.2 Digital Inputs and Outputs, MCLK = 8.192 MHz, f_S = 8 kHz, DV_{DD} = 3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, DOUT	I_O = 360 µA	2.4	3		V
V_{OL}	Low-level output voltage, DOUT	I_O = –2 mA		0.2	0.4	V
I_{IH}	High-level input current, any digital input	V_{IH} = 3 V			10	µA
I_{IL}	Low-level input current, any digital input	V_{IL} = 0.6 V			10	µA
C_i	Input capacitance			5		pF
C_o	Output capacitance			5		pF

4.3.3 ADC Channel, MCLK = 8.192 MHz, f_S = 8 kHz (see Note 4, Figures 5-6 and 5-7)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter gain relative to gain at 1020 Hz	0 to 300 Hz	–0.5		0.2	dB
	300 Hz to 3 kHz	–0.25		0.25	
	3.3 kHz	–0.35		0.3	
	3.6 kHz			–3	
	4 kHz			–40	
	≥ 4.4 kHz			–74	

NOTE 4: The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The analog input test signal is a sine wave with 0 dB = 4 V_{PP} as the reference level for the analog input signal. The passband is 0 to 3600 Hz for an 8-kHz sample rate. This passband scales linearly with the sample rate.

4.3.4 ADC Dynamic Performance, MCLK = 8.192 MHz, f_S = 8 kHz

4.3.4.1 ADC Signal-to-Noise (see Note 5 and Figure 5-10)

PARAMETER	TEST CONDITIONS	TLC320AD50C/52C			TLC320AD50I			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Signal-to-noise ratio (SNR)	V_I = –1 dB (5.35 V)	85	89		83	87		dB
	V_I = –9 dB (2.13 V)	77	81		75	79		
	V_I = –40 dB (60 mV)	46	50		44	48		
	V_I = –65 dB (3 mV)	21	25		19	23		
	V_{AUX} = –9 dB	77	81		75	79		

NOTE 5: The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output are referenced to AV_{DD}/2.

4.3.4.2 ADC Signal-to-Distortion (see Note 5 and Figure 5-11)

PARAMETER	TEST CONDITIONS	TLC320AD50C/52C			TLC320AD50I			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Signal-to-total harmonic distortion (THD)	V_I = –3 dB (4.25 V)	80	85		79	84		dB
	V_I = –9 dB (2.13 V)	79	90		78	89		
	V_I = –40 dB (60 mV)	67	72		66	71		
	V_I = –65 dB (3 mV)	43	48		42	47		
	V_{AUX} = –9 dB	79	90		78	89		

NOTE 5. The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output are referenced to $V_{DD}/2$.

4.3.4.3 ADC Signal-to-Distortion + Noise (see Note 5 and Figure 5-12)

PARAMETER	TEST CONDITIONS	TLC320AD50C/52C			TLC320AD50I			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Signal-to-total harmonic distortion + noise (THD + N)	V_I = –3 dB (4.25 V)	78	82		76	80		dB
	V_I = –9 dB (2.13 V)	76	80		74	78		
	V_I = –40 dB (60 mV)	45	49		43	47		
	V_I = –65 dB (3 mV)	20	24		19	22		
	V_{AUX} = –9 dB	76	80		74	78		

NOTE 5. The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output are referenced to $V_{DD}/2$.

4.3.5 ADC Channel Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(PP)}$	Peak-to-peak input voltage (differential (INP–INM) peak, for full scale operation)				6	V
	Dynamic range	V_I = –1 dB (5.35 V)		88		dB
	Interchannel isolation			100		dB
E_G	Gain error	V_I = –1 dB at 1020 Hz		±0.3		dB
$E_{O(ADC)}$	ADC converter offset error			5	15	mV
CMRR	Common-mode rejection ratio at INM, INP or AUXM, AUXP	V_I = –1 dB at 1020 Hz		74		dB
	Idle channel noise (on-chip reference)	$V_{INP, INM}$ = 2.5 V			75	μV rms
R_i	Input resistance	T_A = 25°C		35		kΩ
	Channel delay			$17/f_S$		s

4.3.6 DAC Path Filter, MCLK = 8.192 MHz, f_S = 8 kHz (see Note 6, Figures 5-8 and 5-9)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter gain relative to gain at 1020 Hz	0 to 300 Hz	–0.5		0.2	dB
	300 Hz to 3 kHz	–0.25		0.25	
	3.3 kHz	–0.35		0.3	
	3.6 kHz			–3	
	4 kHz			–40	
	≥ 4.4 kHz			–74	

NOTE 6: The filter gain outside of the pass band is measured with respect to the gain at 1020 Hz. The input signal is the digital equivalent of a sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 $V_{I(PP)}$. The pass band is 0 to 3600 Hz for an 8-kHz sample rate. This pass band scales linearly with the conversion rate.

4.3.7 DAC Dynamic Performance

4.3.7.1 DAC Signal-to-Noise When Load is 600 Ω (see Note 7 and Figure 5-13)

PARAMETER	TEST CONDITIONS	TLC320AD50C/52C			TLC320AD50I			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Signal-to-noise ratio (SNR)	V_I = 0 dB	85	89		83	87		dB
	V_I = –9 dB	76	80		74	78		
	V_I = –40 dB	45	49		43	47		
	V_I = –65 dB	20	24		18	22		

NOTE 7: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at output of application schematic low-pass filter. The test is conducted in 16-bit mode.

4.3.7.2 DAC Signal-to-Noise When Load is 10 kΩ (see Note 7)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise ratio (SNR)	V_I = 0 dB		89		dB
	V_I = –9 dB		80		
	V_I = –40 dB		50		
	V_I = –65 dB		25		

NOTE 7: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at output of application schematic low-pass filter. The test is conducted in 16-bit mode.

4.3.7.3 DAC Signal-to-Distortion When Load is 600 Ω (see Note 7, Figure 5-14)

PARAMETER	TEST CONDITIONS	TLC320AD50C/52C			TLC320AD50I			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Signal-to-total harmonic distortion (THD)	V_I = –3 dB	76	80		74	78		dB
	V_I = –9 dB	84	90		82	88		
	V_I = –40 dB	64	72		62	70		
	V_I = –65 dB	42	48		40	46		

NOTE 7: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at output of application schematic low-pass filter. The test is conducted in 16-bit mode.

4.3.7.4 DAC Signal-to-Distortion When Load is 10 kΩ (see Note 7)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-total harmonic distortion (THD)	V_I = –3 dB		82		dB
	V_I = –9 dB		91		
	V_I = –40 dB		77		
	V_I = –65 dB		49		

NOTE 7: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at output of application schematic low-pass filter. The test is conducted in 16-bit mode.

4.3.7.5 DAC Signal-to-Distortion+Noise When Load is 600 Ω (see Note 7, Figure 5-15)

PARAMETER	TEST CONDITIONS	TLC320AD50C/52C			TLC320AD50I			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Signal-to-total harmonic distortion + noise (THD + N)	V_I = –3 dB	75	79		72	76		dB
	V_I = –9 dB	75	79		72	76		
	V_I = –40 dB	45	49		42	46		
	V_I = –65 dB	20	24		17	21		

NOTE 7: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at output of application schematic low-pass filter. The test is conducted in 16-bit mode.

4.3.8 DAC Channel Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Dynamic range			88		dB
	Interchannel isolation			100		dB
E_G	Gain error, 0 dB	V_O = 0 dB at 1020 Hz		±0.3		dB
	Idle channel narrow band noise	0 – 4 kHz, See Note 8			125	μV rms
V_{OO}	Output offset voltage at OUT (differential)	DIN = All 0s		30		mV
V_O	Analog output voltage, OUTP – OUTM	R_L = 600 Ω typ (see Figure 2–17) with internal reference and full-scale digital input, See Note 9, differential			6	V_{PP}
	Total out of band energy (0.55 f_S to 3 MHz)				–45	dB
	Channel delay			$18/f_S$		

NOTES: 8. The conversion rate is 8 kHz; the-out-of-band measurement is made from 4400 Hz to 3 MHz.
9. The digital input to the DAC channel at DIN is in 2s complement format. The TLC320AD50C/52C DAC is of the voltage-type and requires a load resistor for current to voltage conversion.

4.3.9 Power Supply, AV_{DD} = DV_{DD} = 5 V, No Load

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD} (analog)	Power supply current, ADC	Operating		18	24	mA
		Power down		1		
I_{DD} (PLL)	Power supply current, PLL	Operating		2	4	mA
		Power down		0.5		
I_{DD} (digital 1)	Power supply current, digital	Operating		4	6	mA
		Power down		10		μA
I_{DD} (digital 2)	Power supply current, digital, DV_{DD} = 3 V	Operating		4		mA
		Power down		10		μA
P_D	Power dissipation	Operating		120	170	mW
		H/W-power down		7.5	20	

4.3.10 Power-Supply Rejection, AV_{DD} = DV_{DD} = 5 V (see Note 10)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AV_{DD}	Supply voltage rejection ratio, analog supply	f_i = 0 to $f_S/2$		50		dB
DV_{DD}	Supply voltage rejection ratio, DAC channel	f_i = 0 to 30 kHz		40		
DV_{DD}	Supply voltage rejection ratio, ADC channel	f_i = 0 to 30 kHz		50		

NOTE 10: Power supply rejection measurements are made with both the ADC and the DAC channels idle and a 200-mV peak-to-peak signal applied to the appropriate supply.

4.4 Timing Characteristics (see Parameter Measurement Information)

4.4.1 Master Mode Timing Requirements

		MIN	NOM	MAX	UNIT
t_{d1}	Delay time, SCLK↑ to $\overline{FS}$↓			0	ns
t_{su1}	Setup time, DIN, before SCLK low	25			
t_{h1}	Hold time, DIN, after SCLK low			20	
$t_{d(CH–FDL)}$	Delay time, SCLK high to $\overline{FSD}$ low (see Figure 5–1)			50	
t_{wH}	Pulse duration, MCLK high	32			
t_{wL}	Pulse duration, MCLK low	20			

4.4.2 Slave Mode Timing Requirements

		MIN	NOM	MAX	UNIT
t_{d4}	Delay time, SCLK↑ to $\overline{FS}$↓			0	ns
t_{su2}	Setup time, DIN, before SCLK low	20			
t_{h2}	Hold time, DIN, after SCLK low			20	
$t_{d(FL–FDL)}$	Delay time, $\overline{FS}$ low to $\overline{FSD}$ low, (see Figure 5–2)			40	
$t_{d(CH–FDL)}$	Delay time, SCLK high to $\overline{FSD}$ low, slave mode (see Figure 5–3)			50	
t_{wH}	Pulse duration, MCLK high	32			
t_{wL}	Pulse duration, MCLK low	20			

4.4.3 Master Mode Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d2}	Delay time, SCLK↑ to DOUT	C_L = 20 pF			20	ns
t_{en1}	Enable time, $\overline{FS}$↓ to DOUT				25	
t_{dis1}	Disable time, $\overline{FS}$↑ to DOUT Hi-Z			20		

4.4.4 Slave Mode Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d5}	Delay time, SCLK↑ to DOUT	C_L = 20 pF			20	ns
t_{en2}	Enable time, $\overline{FS}$↓ to DOUT				25	
t_{dis2}	Disable time, $\overline{FS}$↑ to DOUT Hi-Z			20		

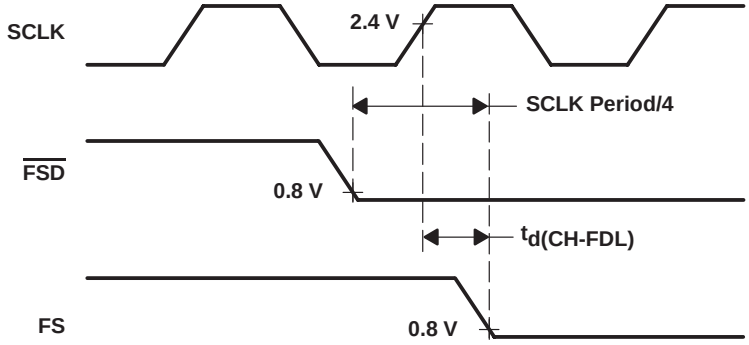
4.4.5 Reset Timing

PARAMETER		MIN	TYP	MAX	UNIT
t_{PW}	Reset pulsewidth	6 MCLKs			ns

4.4.6 Other

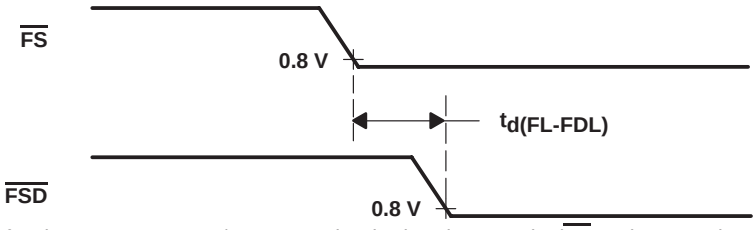
PARAMETER		MIN	TYP	MAX	UNIT
t_{su3}	Setup time, FC before FS↑	10			ns
t_{h3}	Hold time, FC after FS↑	10			ns

5 Parameter Measurement Information



NOTE A: Timing shown is for the TLC320AD50C/52C operating as the master device. The programmed data value in the FSD register is 0. D0 through D5 of control 3 register are all 0.

Figure 5–1. Master $\overline{FS}$ and $\overline{FSD}$ Timing

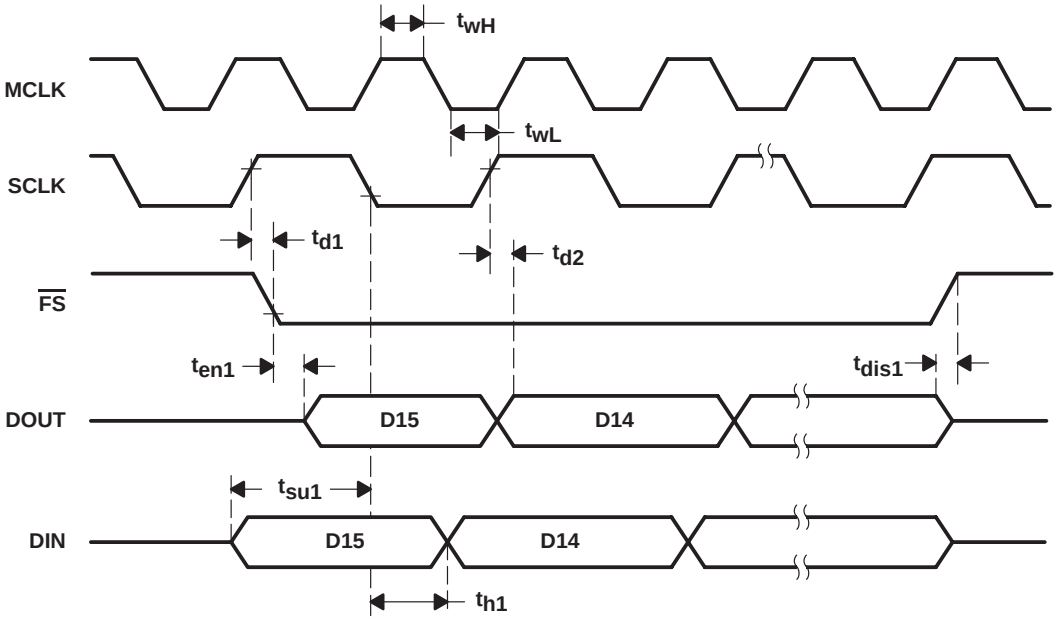


NOTE A: Timing shown is for the TLC320AD50C/52C operating in the slave mode ($\overline{FS}$ and SCLK signals are generated externally). The programmed data value in the FSD register is 0.

Figure 5–2. Slave $\overline{FS}$ to $\overline{FSD}$ Timing

NOTE A: Timing shown is for the TLC320AD50C/52C operating in the slave mode ($\overline{FS}$ and SCLK signals are generated externally). There is a data value in the FSD register greater than 18 decimal. D0 through D5 of control 3 register are greater than 17.

Figure 5–3. Master/Slave SCLK to $\overline{FSD}$ Timing



NOTE A: The master mode and D0 through D5 of control 3 register are greater than 17.

Figure 5–4. Serial Communication Timing (Master Mode)

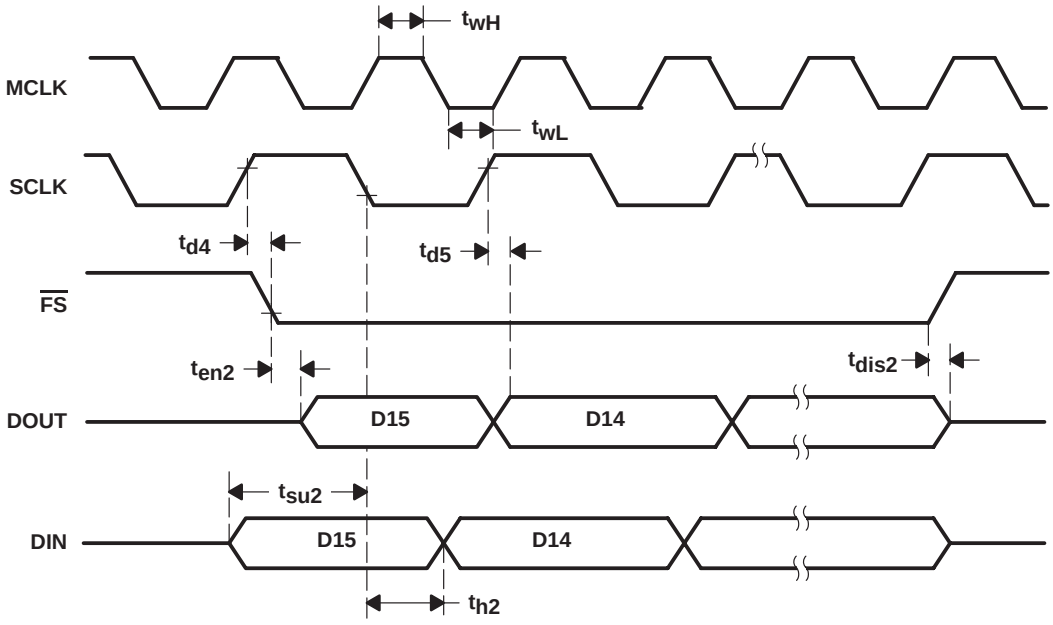


Figure 5–5. Serial Communication Timing (Slave Mode)

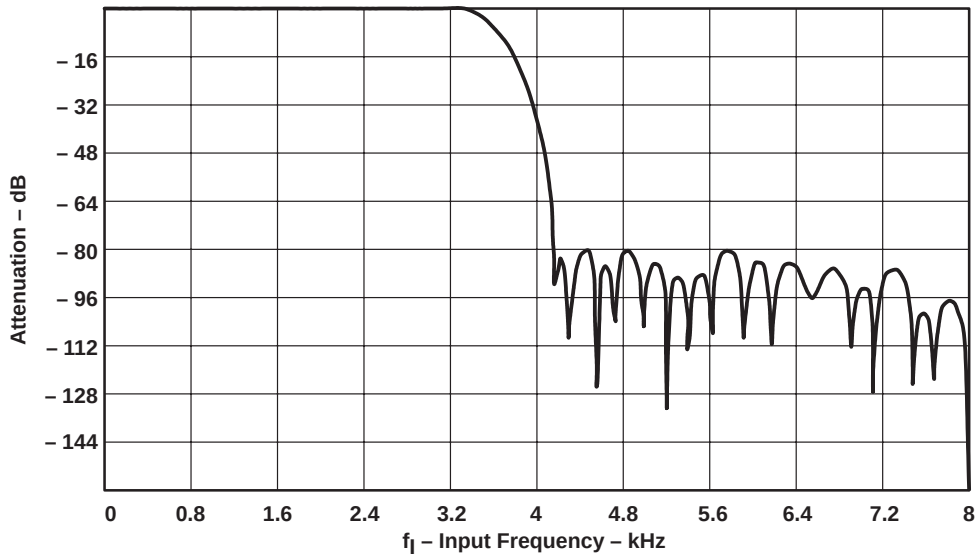


Figure 5–6. ADC Channel Filter Response (MCLK = 8.192 MHz, f_S = 8 kHz)

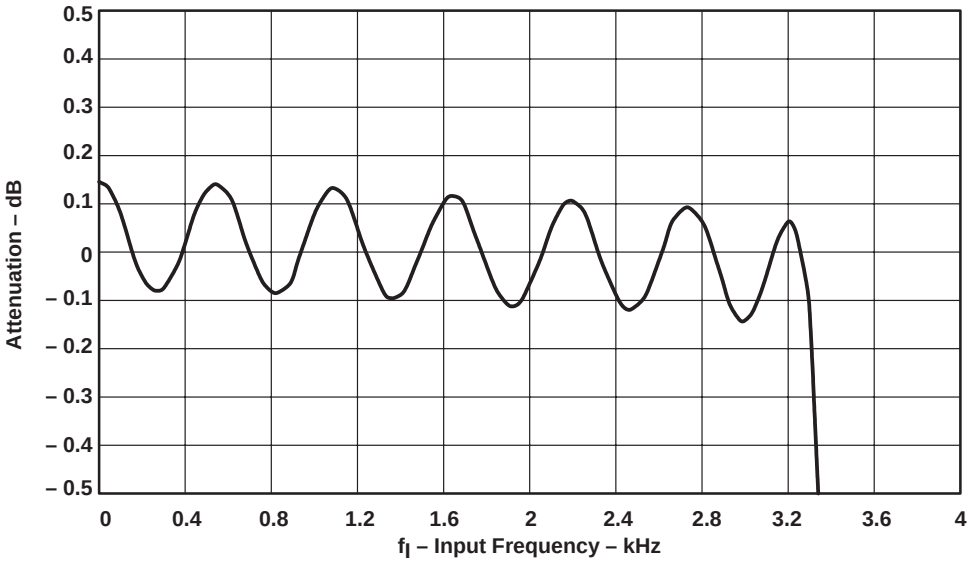


Figure 5–7. ADC Channel Filter Passband Ripple (MCLK = 8.192 MHz, f_S = 8 kHz)

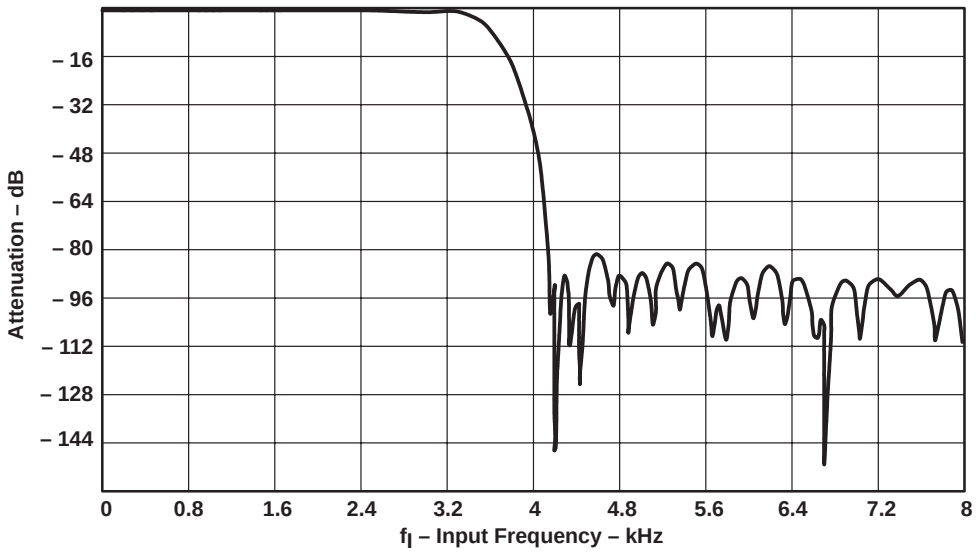


Figure 5–8. DAC Channel Filter Response (MCLK = 8.192 MHz, f_S = 8 kHz)

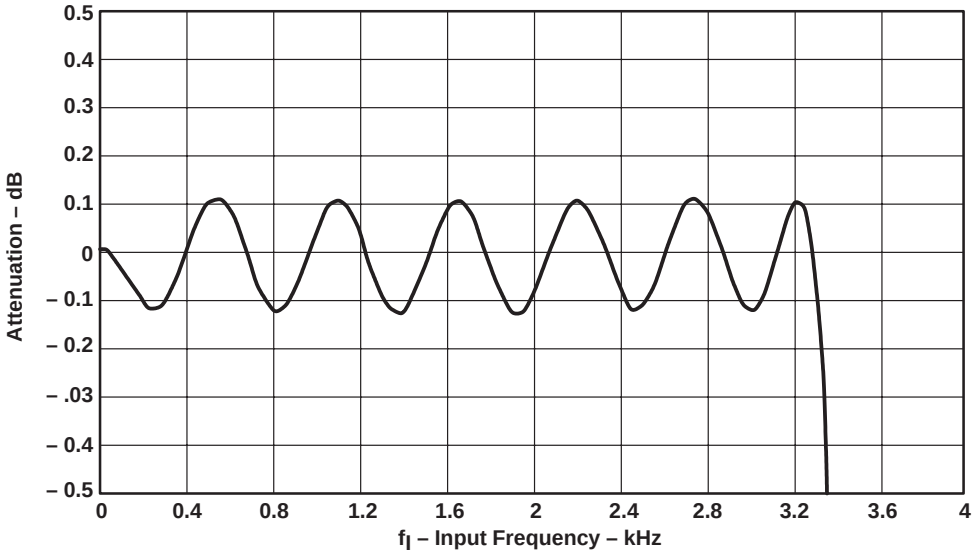


Figure 5–9. DAC Channel Filter Passband Ripple (MCLK = 8.192 MHz, f_S = 8 kHz)

ADC SIGNAL-TO-NOISE RATIO
vs
INPUT SIGNAL

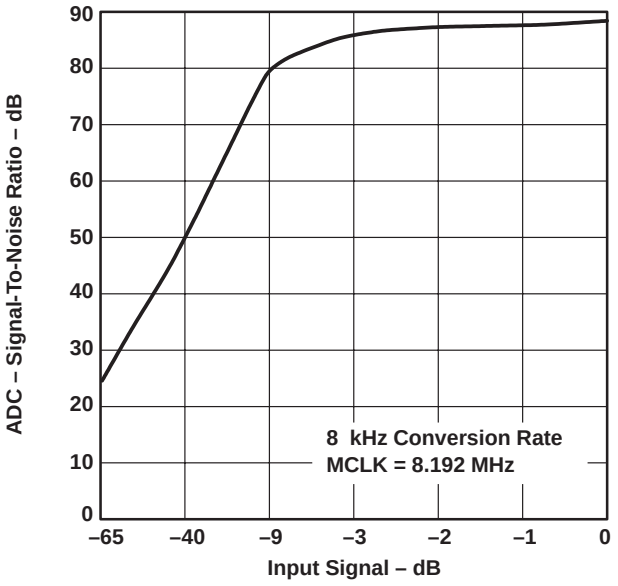


Figure 5–10

ADC SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL

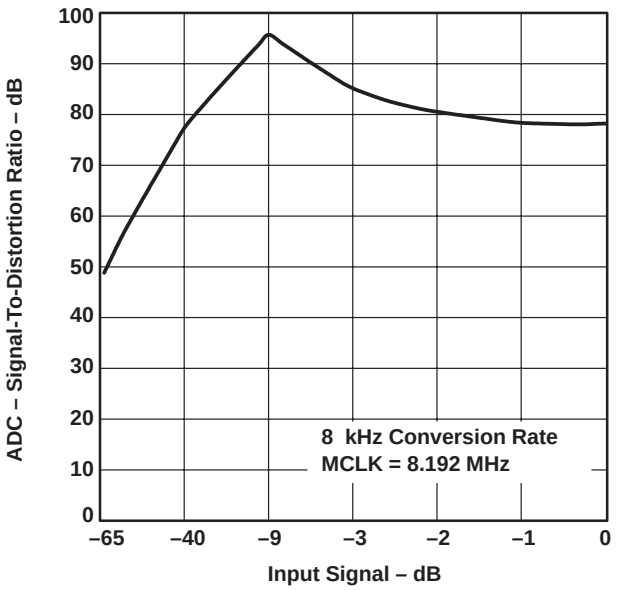


Figure 5–11

ADC SIGNAL-TO-(NOISE AND DISTORTION) RATIO
vs
INPUT SIGNAL

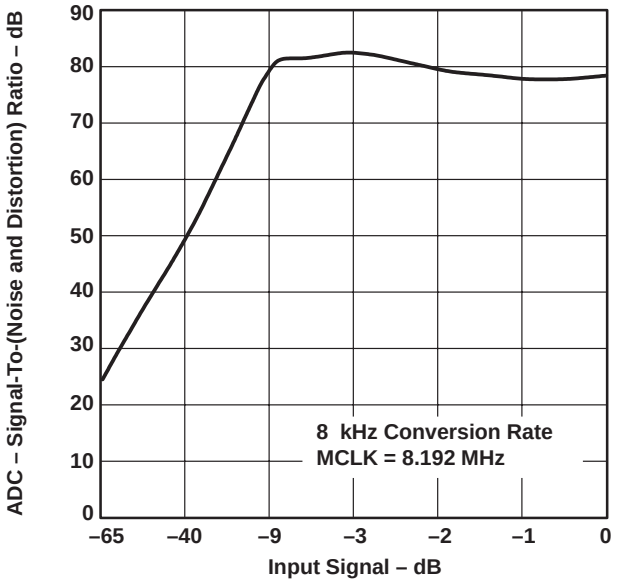


Figure 5–12

DAC SIGNAL-TO-NOISE RATIO
vs
INPUT SIGNAL

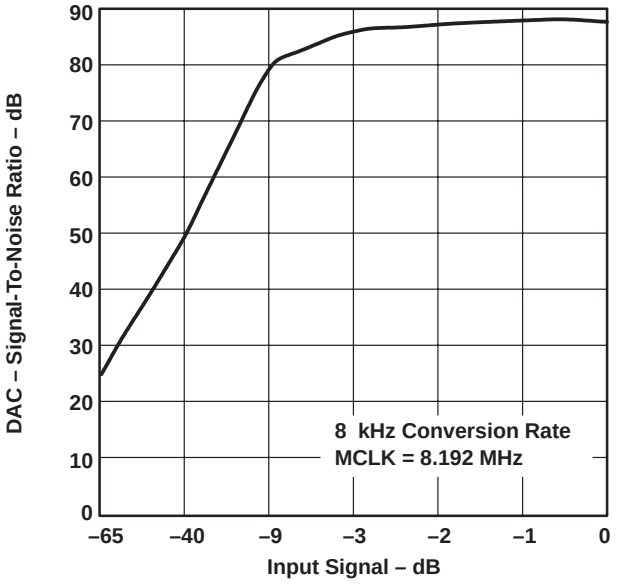


Figure 5–13

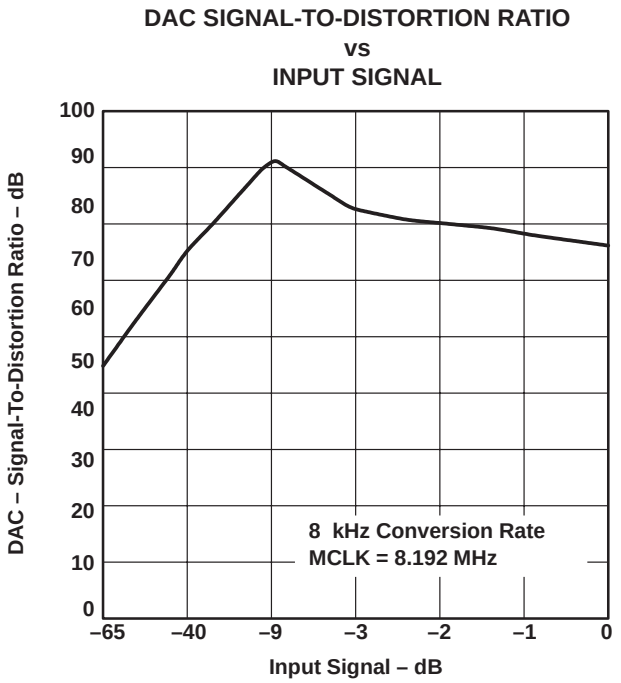


Figure 5–14

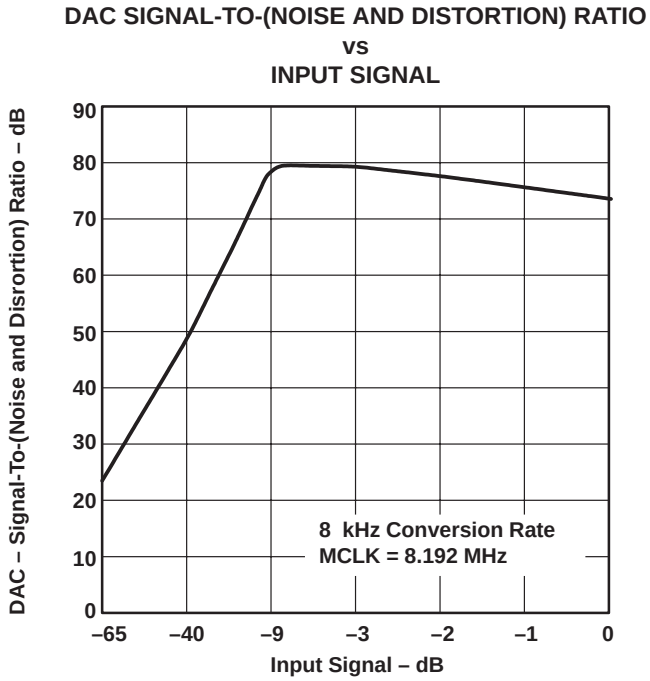


Figure 5–15

6 Register Set

Bits D12 through D8 in a secondary serial communication comprise the address of the register that is written with data carried in D7 through D0. D13 determines a read or write cycle to the addressed register. When low, a write cycle is selected.

The following table shows the register map.

Table 6–1. Register Map

REGISTER NO.	D15	D14	D13	D12	D11	D10	D9	D8	REGISTER NAME
0	0	0	0	0	0	0	0	0	No operation
1	0	0	0	0	0	0	0	1	Control 1
2	0	0	0	0	0	0	1	0	Control 2
3	0	0	0	0	0	0	1	1	Control 3
4	0	0	0	0	0	1	0	0	Control 4

6.1 Control Register 1

Table 6–2. Control Register 1

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1	–	–	–	–	–	–	–	Software reset
0	–	–	–	–	–	–	–	Software reset not asserted
–	1	–	–	–	–	–	–	Software power down (analog and filters)
–	0	–	–	–	–	–	–	Software power down (not asserted)
–	–	1	–	–	–	–	–	Select AUXP and AUXM for ADC
–	–	0	–	–	–	–	–	Select INP and INM for ADC
–	–	–	0	–	–	–	–	Select INP and INM for monitor
–	–	–	1	–	–	–	–	Select AUXP and AUXM for monitor
–	–	–	–	1	1	–	–	Monitor amplifier gain = –18 dB (see Note 1)
–	–	–	–	1	0	–	–	Monitor amplifier gain = –8 dB (see Note 1)
–	–	–	–	0	1	–	–	Monitor amplifier gain = 0 dB (see Note 1)
–	–	–	–	0	0	–	–	Monitor amp mute
–	–	–	–	–	–	1	–	Digital loopback asserted
–	–	–	–	–	–	0	–	Digital loopback not asserted
–	–	–	–	–	–	–	1	16-bit DAC mode (hardware secondary requests)
–	–	–	–	–	–	–	0	Not 16-bit DAC mode (software secondary requests) [(15+1)– bit mode]

Default value: 0 0 0 0 0 0 0 0

NOTE 1: These gains are for a single-ended input. The gain is 6 dB lower with a differential input.

A software reset is a one-shot operation and this bit is cleared to 0 after reset. It is not necessary to write a 0 to end the master reset operation. Writing 0s to the reserved bits is suggested.

6.2 Control Register 2

Table 6–3. Control Register 2

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
X	–	–	–	–	–	–	–	FLAG output value
–	1	–	–	–	–	–	–	Phone mode enable
–	0	–	–	–	–	–	–	Phone mode disable
–	–	X	–	–	–	–	–	Decimator FIR overflow flag (valid only during read cycle)
–	–	–	1	–	–	–	–	16-bit ADC mode
–	–	–	0	–	–	–	–	Not-16-bit ADC mode [(15+1)– bit mode]
–	–	–	–	–	X	0	0	Reserved (TLC320AD50C only)
–	–	–	–	–	0	0	0	$\overline{\text{FSD}}$ enable (TLC320AD52C only)
–	–	–	–	–	1	–	–	$\overline{\text{FSD}}$ disable (TLC320AD52C only)
–	–	–	–	1	–	–	–	Analog loopback enabled
–	–	–	–	0	–	–	–	Analog loopback disabled

Default value: 00000000

Writing 0s to the reserved bits is suggested.

6.3 Control Register 3

The following command contains the frame-sync delay (FSD) register address and loads D7 (MSB)–D0 into the FSD register. The data byte (D5–D0) determines the number of SCLKs between $\overline{\text{FS}}$ and the delayed frame-sync signal, $\overline{\text{FSD}}$. The minimum data value for this portion of the register, bits D5–D0, is decimal 18.

Table 6–4. Control Register 3

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
–	–	X	X	X	X	X	X	Number of SCLKs between $\overline{\text{FS}}$ and $\overline{\text{FSD}}$
X	X	–	–	–	–	–	–	Binary number of slave devices (3 maximum for TLC320AC50C, 1 maximum for TLC320AC52C)

Default value: 00000000

Writing 0s to the reserved bits is suggested.

6.4 Control Register 4

Table 6–5. Control Register 4

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
–	–	–	–	1	1	–	–	Analog input gain = mute
–	–	–	–	1	0	–	–	Analog input gain = 12 dB
–	–	–	–	0	1	–	–	Analog input gain = 6 dB
–	–	–	–	0	0	–	–	Analog input gain = 0 dB
–	–	–	–	–	–	1	1	Analog output gain = mute
–	–	–	–	–	–	1	0	Analog output gain = – 12 dB
–	–	–	–	–	–	0	1	Analog output gain = – 6 dB
–	–	–	–	–	–	0	0	Analog output gain = 0 dB
–	X	X	X	–	–	–	–	Sample frequency select (N): f_S = MCLK/(128 $\times$ N) or MCLK/(512 $\times$ N)
1	–	–	–	–	–	–	–	Bypass internal DPLL
0	–	–	–	–	–	–	–	Enable internal DPLL

Default value: 00000000

The value of the sample frequency divisor, N, is determined by the octal representation of bits D4–D6. Hence, 001 = 1, 010 = 2, etc. By setting D4–D6 to 000, N = 8 is selected.

7 Application Information

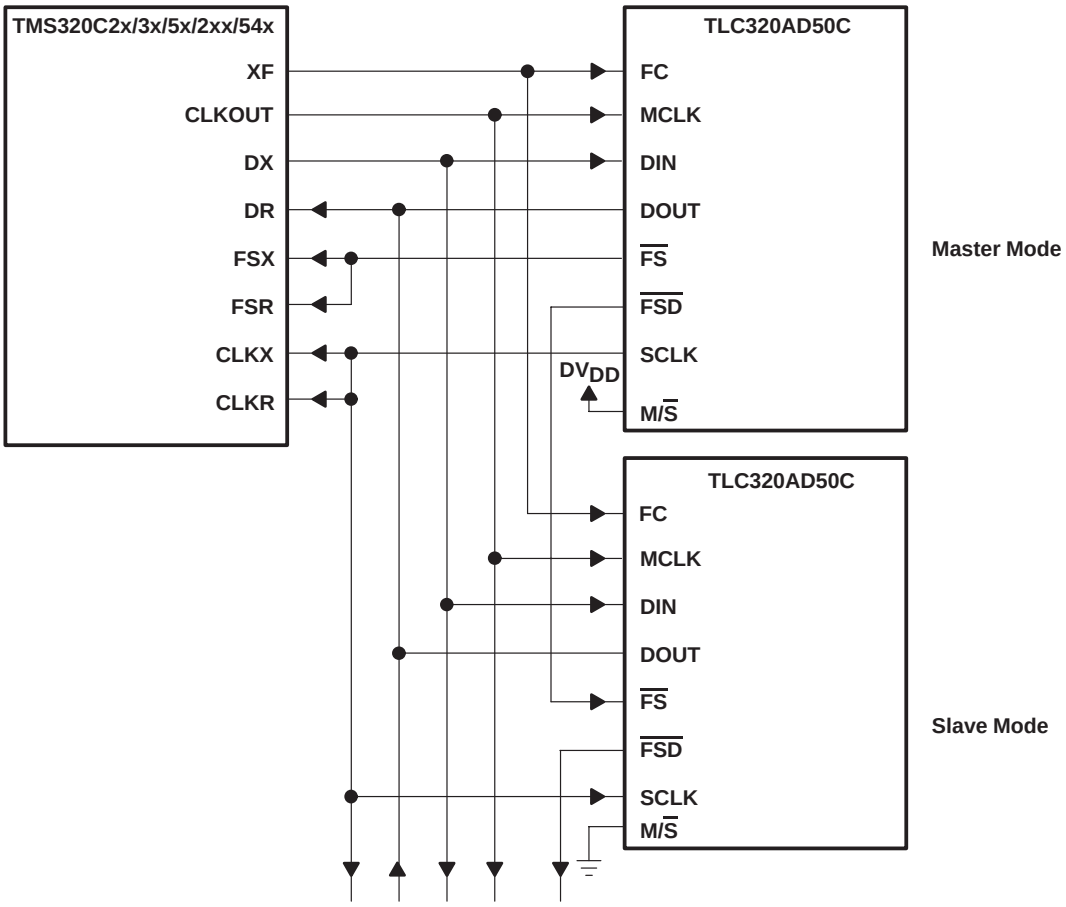


Figure 7–1. Master Device and Slave Device Connections (to DSP Interface)

When multiple AD50's or AD52's are attached to a single DSP serial interface in a master/slave configuration, the control registers should be programmed in the following order during device initialization:

Control register 1
Control register 2
Control register 4
Control register 3

All AD50 or AD52 devices will be configured the same with a single global initialization being written to registers 1, 2, and 4. Once register 3 is programmed (setting the number of SCLKS between FS and FSD), each device will begin communicating in its designated time slot.

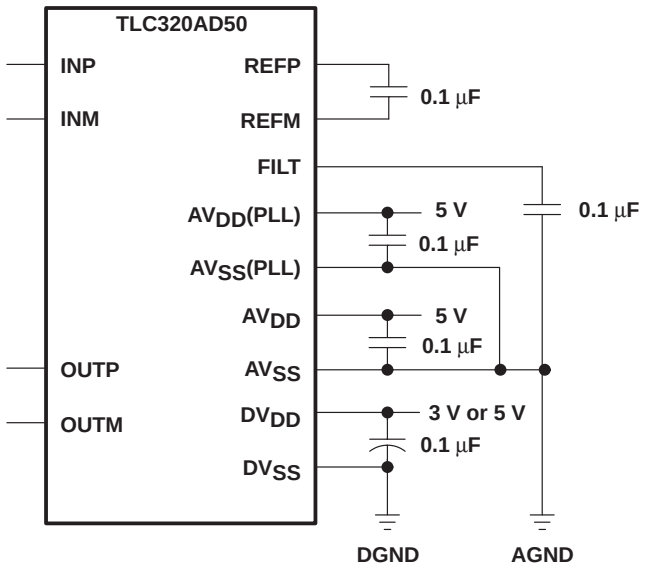


Figure 7–2. Power Supply Decoupling

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC320AD50CDW	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC320AD50C	Samples
TLC320AD50CPT	ACTIVE	LQFP	PT	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		P320AD50	Samples
TLC320AD50CPTR	ACTIVE	LQFP	PT	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		P320AD50	Samples
TLC320AD50IDW	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC320AD50I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

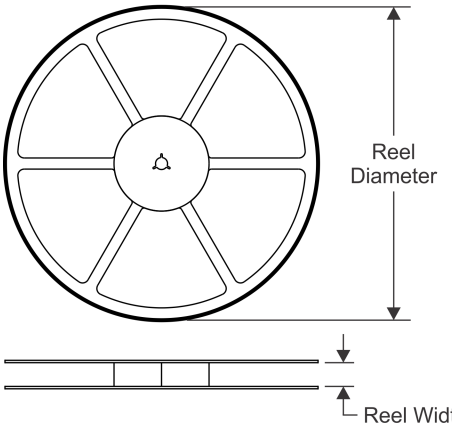
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

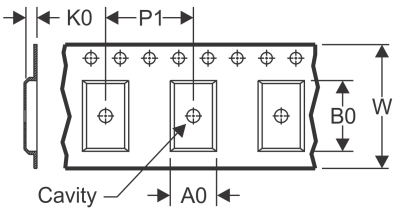
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

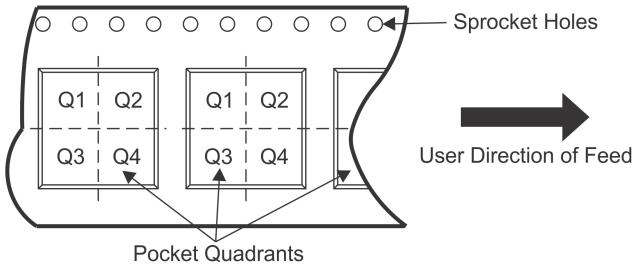


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

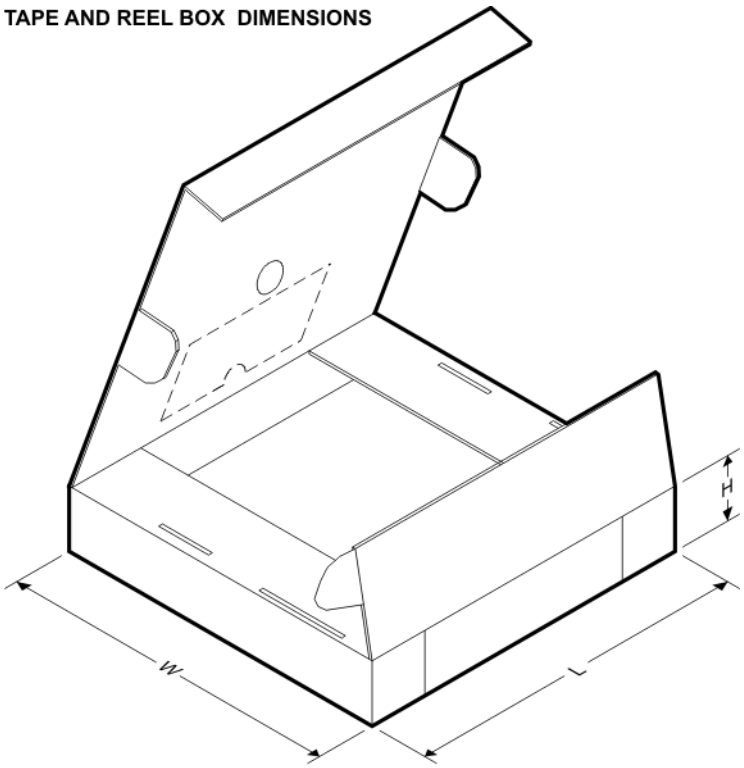
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC320AD50CPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

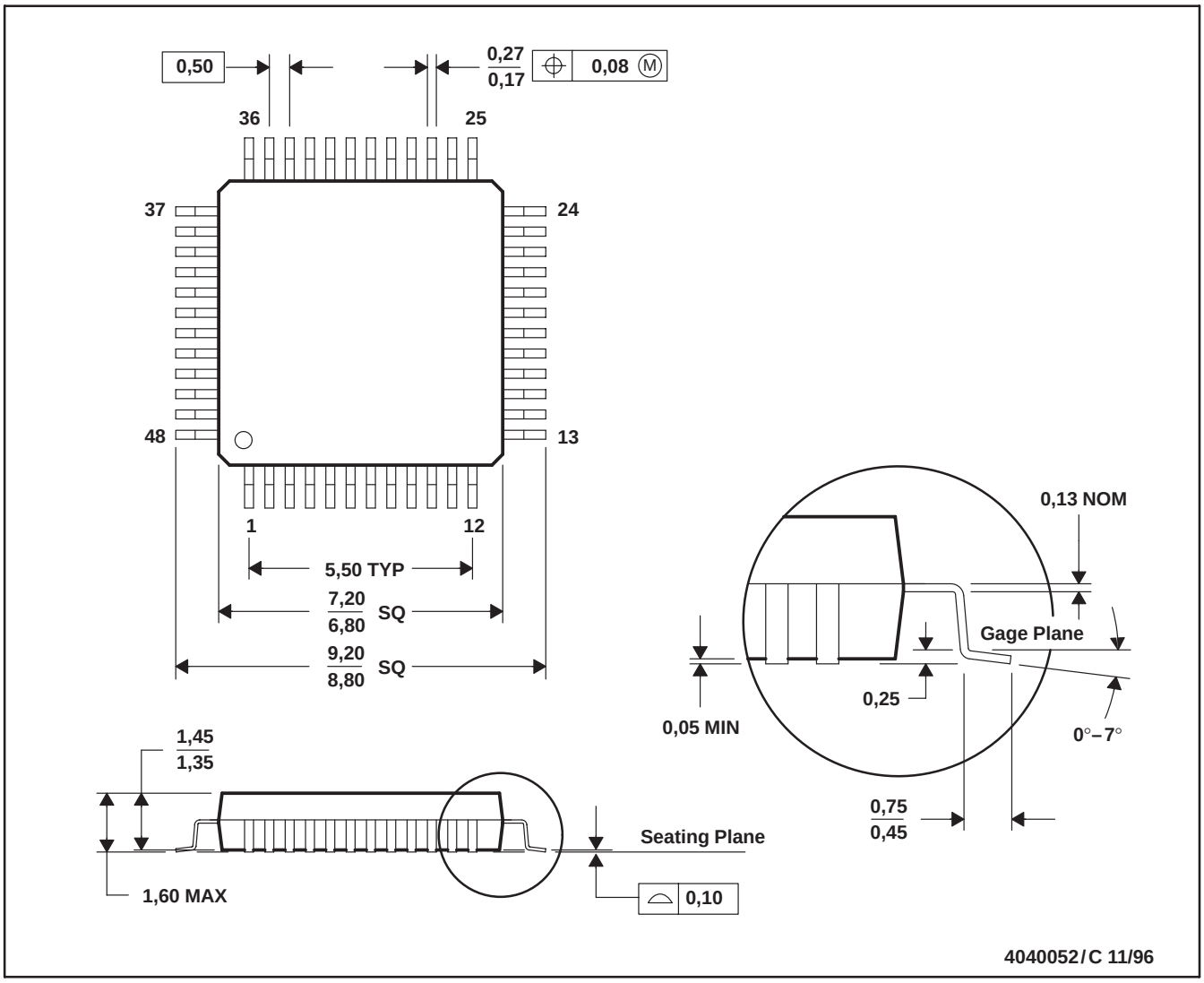


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC320AD50CPTR	LQFP	PT	48	1000	367.0	367.0	38.0

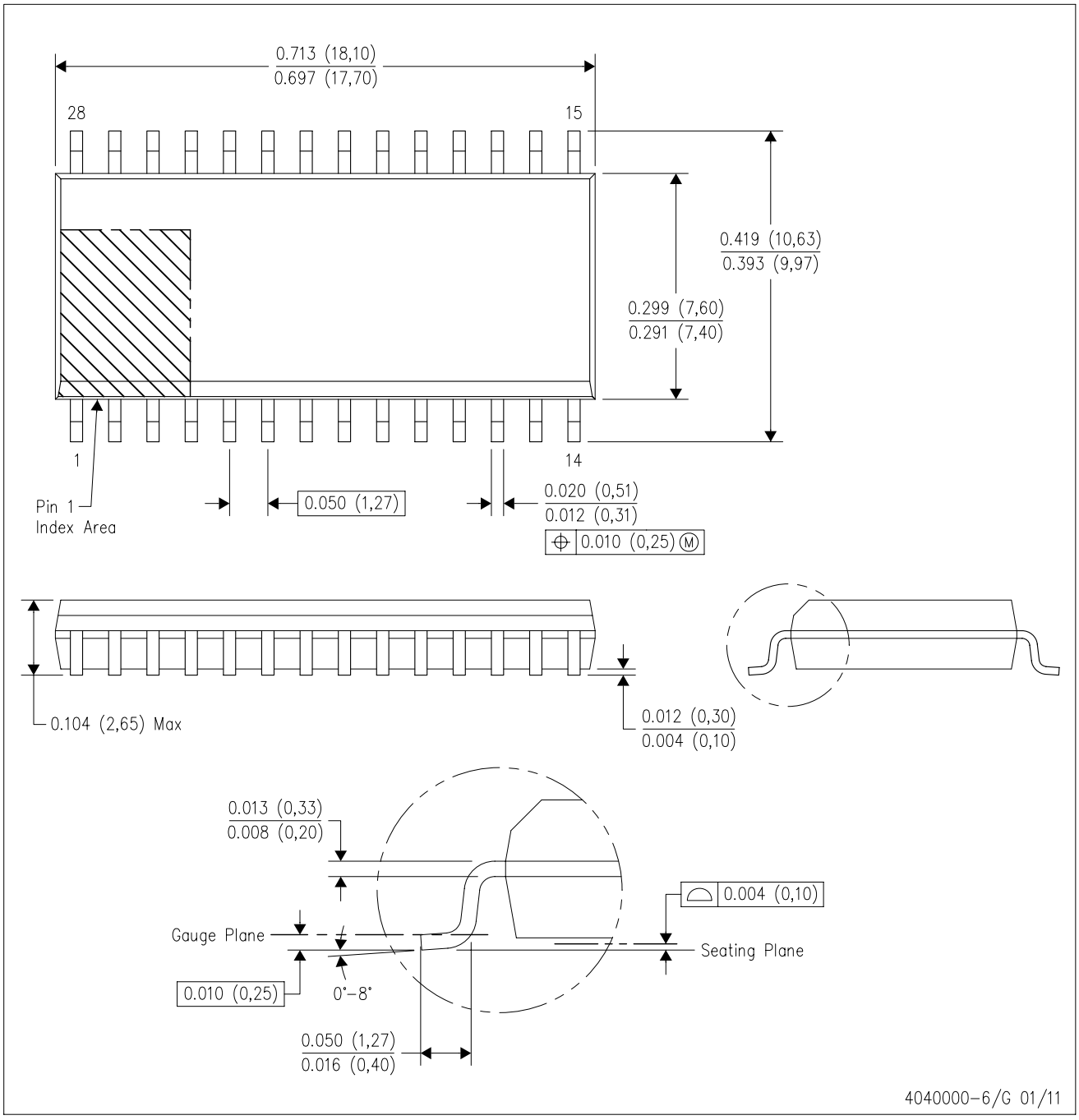
MTQF003A – OCTOBER 1994 – REVISED DECEMBER 1996

PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



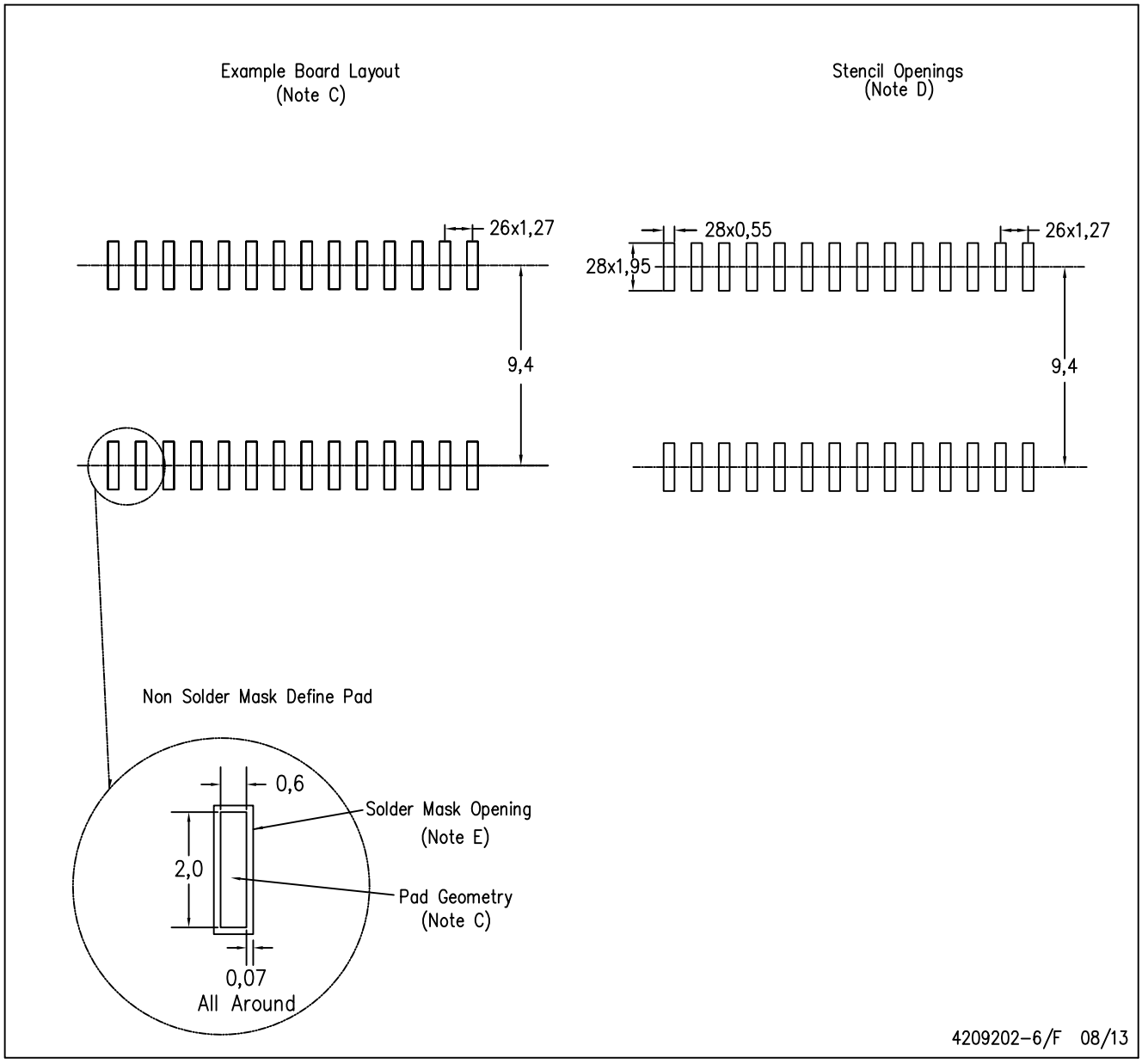
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. This may also be a thermally enhanced plastic package with leads conected to the die pads.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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